# LT8918 --- Product Brief

# RGB/LVDS to MIPI DSI/CSI-2 with MIPI Repeater

## Features

- **RGB Input**
  - Support 24-bit RGB and BT656/BT1120 Input
  - Support both SDR and DDR Data Sampling
  - Programmable Rising/Falling Edge Clock Input
  - Support up to 74.25MHz DDR or 148.5MHz SDR Clock Input
  - Support both 1.8V and 3.3V Input Voltage Level
- **Single/Dual-Port LVDS Receiver**
  - Compatible with VESA and JEIDA standard
  - 1~2 Configurable Port
  - 1 Clock Lane and Up to 5 Data Lanes per Port
  - Data Lane and Polarity Swapping
  - Support Maximum Data Rate 1.2Gb/s/lane
  - Resolution Up to 1080P 60Hz for Dual-Port Mode
  - Input Color Depth Supports 6-bit, 8-bit and 10-bit
  - Support Input De-SSC (30kHz±5%)
- **Single-Port MIPI DSI Transmitter**
  - Compliant with DCS1.02, D-PHY1.1 & DSI1.02
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - 80Mb/s~1.5Gb/s per Data Lane
  - Resolution Up to 1080P 60Hz
  - Data Lane and Polarity Swapping
  - Both Non-Burst and Burst Video Mode Supported
  - Command Mode through Lane-0 Supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format
- **Single-Port MIPI CSI-2 Transmitter**
  - Compliant with D-PHY1.1 & CSI-2 1.0
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - 80Mb/s~1.5Gb/s per Data Lane
  - Resolution Up to 1080P 60Hz
  - Data Lane and Polarity Swapping
  - Support RGB565, RGB666, RGB888, 8-bit YUV422 Video Format
- **MIPI DSI/CSI-2 Repeater**
  - Support 3-bit Maximum 10dB Input Equalization
  - Signal Re-driving without Data De-Packetize
  - Input Data Lane and Polarity Swapping
  - 80Mb/s~1.5Gb/s per Data Lane for Both Input and Output
- **Miscellaneous**
  - 1.8V Single Supply Power
  - Support 100KHz and 400KHz I2C slave
  - Support SPI slave
  - External 25MHz Crystal Reference Clock
  - Temperature Range: -40$^0$C ~ +85$^0$C
  - Packaged in QFN64 7.5mm x 7.5mm and BGA81 5mm x 5mm.

## Description

The Lontium LT8918 is a high performance LVDS or parallel RGB to MIPI DSI/CSI-2 bridge chip between AP and mobile display panel or camera .

The RGB input of LT8918 supports both 24-bit and BT656/1120 video format under either SDR or DDR sampling. The maximum input pixel clock frequency is SDR 148.5MHz or DDR 74.25MHz for 1080P@60Hz high-end mobile display or video capture application.

When input is LVDS, LT8918 can be configured as single-port or dual-port with optional De-SSC function. The bridge deserilizes input LVDS data, decodes packets and converts the formatted video data stream to MIPI DSI/CSI-2 transmitter output.

For MIPI DSI/CSI-2 output, LT8918 features a single port MIPI DSI or CSI-2 transmitter with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 1.5Gb/s/lane, which can support a total bandwidth of up to 6Gb/s. LT8918 supports both Non-Burst and Burst DSI video data transferring, as

well as Command Mode throught Lane-0.

# Application

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Tablet PC, Notebook PC
- Car Display and Camera System

# Block Diagram

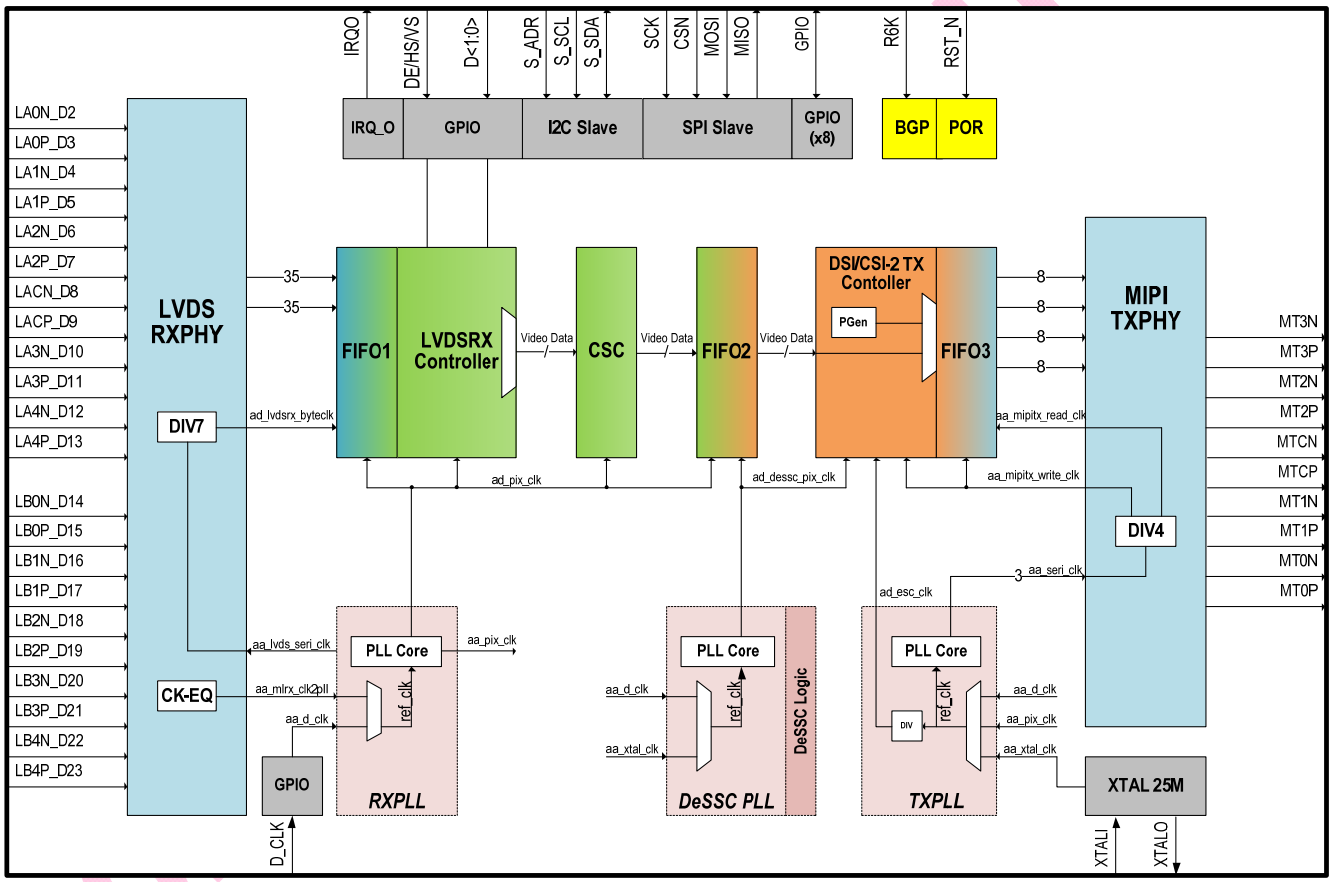



**Fig1 RGB/LVDS-to-MIPI DSI/CSI-2 Functional Diagrams**

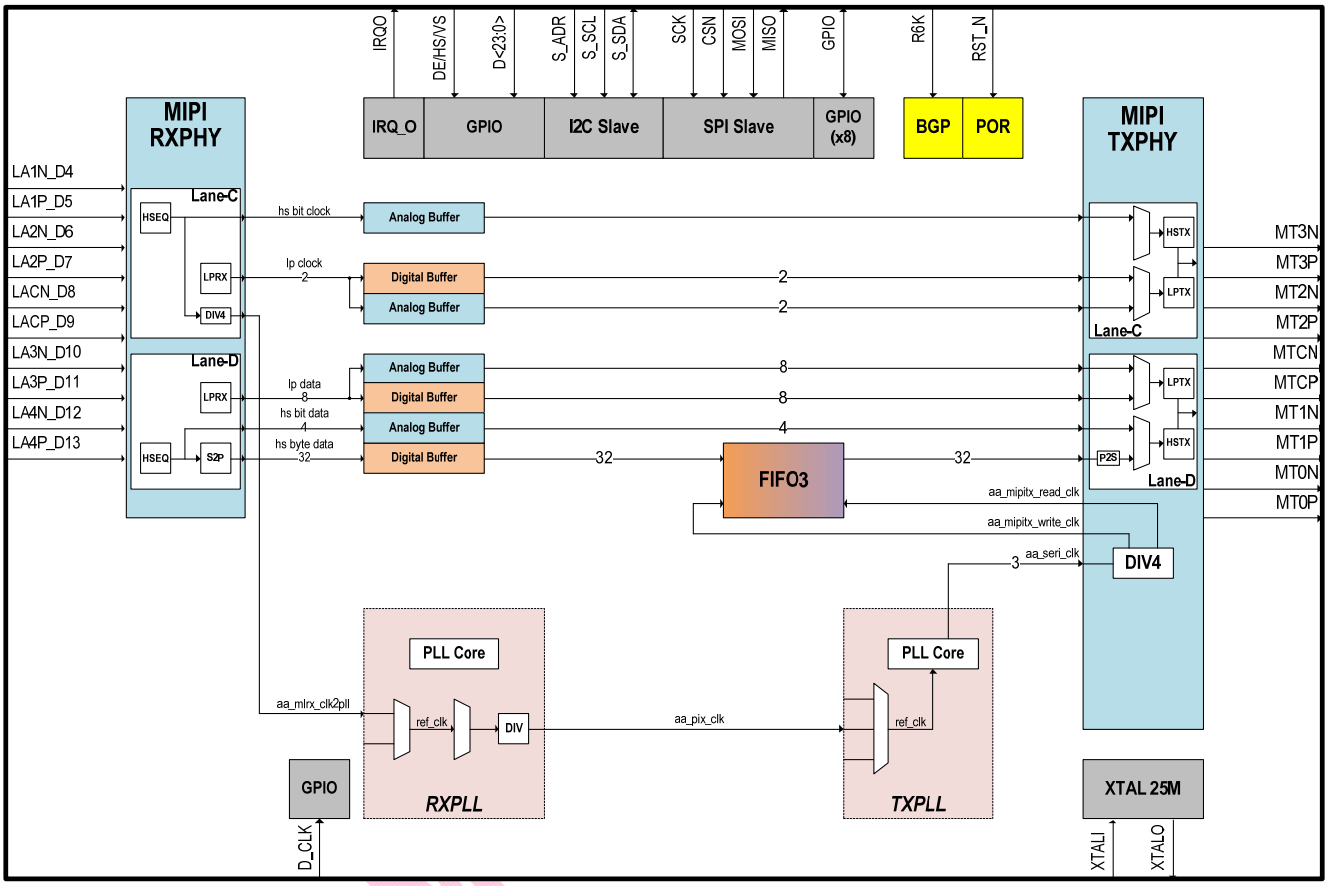
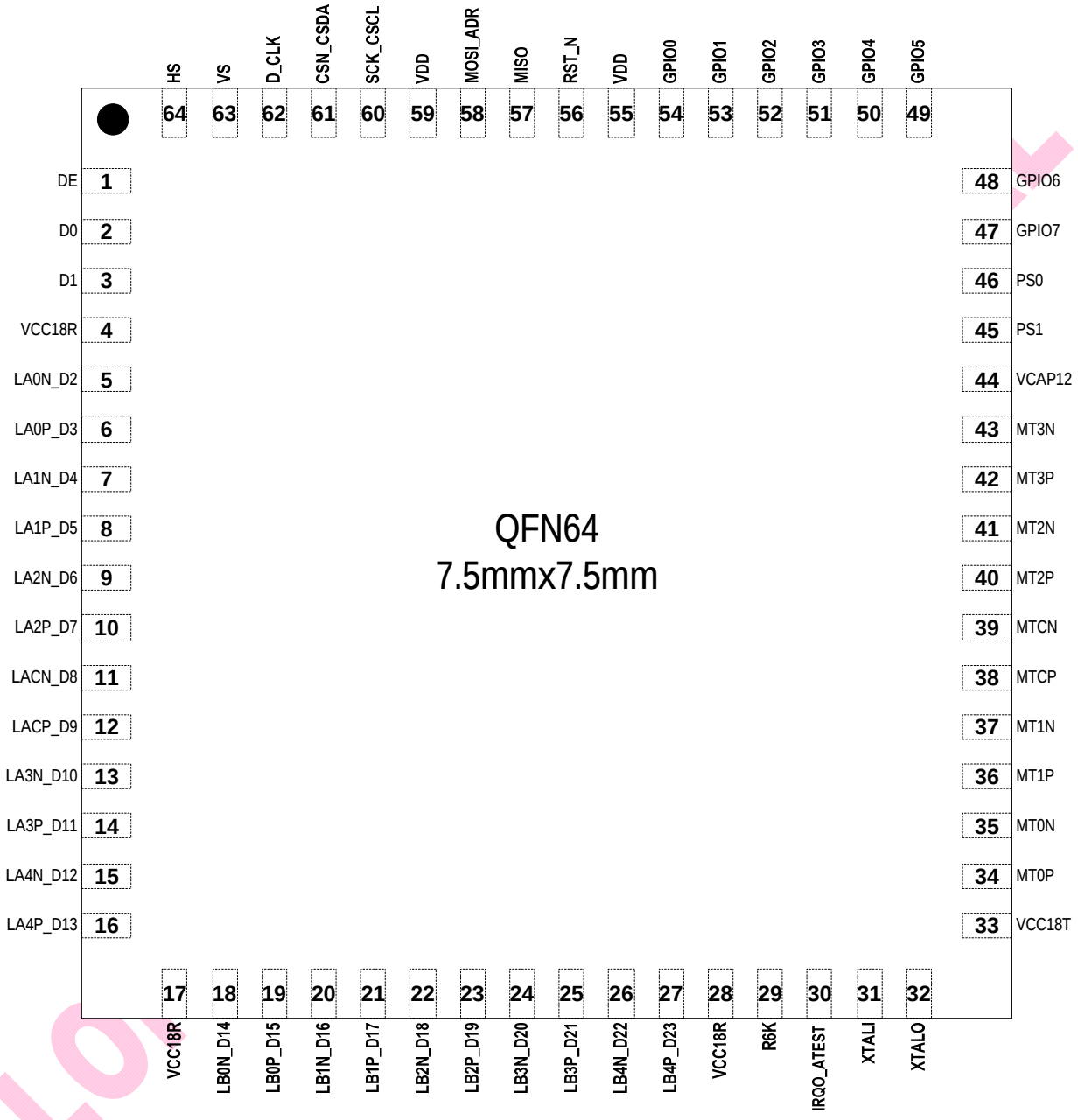



**Fig2 MIPI DSI/CSI-2 Repeater Functional Diagrams**

# Pin Diagram


HS 64
VS 63
D_CLK 62
CSN_CSDA 61
SCK_CSCL 60
VDD 59
MOSI_ADR 58
MISO 57
RST_N 56
VDD 55
GPIO0 54
GPIO1 53
GPIO2 52
GPIO3 51
GPIO4 50
GPIO5 49
DE 1
D0 2
D1 3
VCC18R 4
LA0N_D2 5
LA0P_D3 6
LA1N_D4 7
LA1P_D5 8
LA2N_D6 9
LA2P_D7 10
LACN_D8 11
LACP_D9 12
LA3N_D10 13
LA3P_D11 14
LA4N_D12 15
LA4P_D13 16
48 GPIO6
47 GPIO7
46 PS0
45 PS1
44 VCAP12
43 MT3N
42 MT3P
41 MT2N
40 MT2P
39 MTCN
38 MTCP
37 MT1N
36 MT1P
35 MT0N
34 MT0P
33 VCC18T
17 VCC18R
18 LB0N_D14
19 LB0P_D15
20 LB1N_D16
21 LB1P_D17
22 LB2N_D18
23 LB2P_D19
24 LB3N_D20
25 LB3P_D21
26 LB4N_D22
27 LB4P_D23
28 VCC18R
29 R6K
30 IRQO_ATEST
31 XTALI
32 XTALO
QFN64
7.5mmx7.5mm

# Pin Definition

| Pin No. | Pin Name | Pin Description |
|---|---|---|
| 1 | DE | RGB Data Active Input<br>1.8V/3.3V GPI input with internal 100K pull-down resistor. |
| 2 | D0 | RGB Data Input Bit-0<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 3 | D1 | RGB Data Input Bit-1<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 4 | VCC18R | Analog 1.8V Power<br>1.8V power for LVDS Receiver Port-1 |
| 5 | LA0N_D2 | LVDS Data Lane-0 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-2<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 6 | LA0P_D3 | LVDS Data Port-A Lane-0 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-3<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 7 | LA1N_D4 | LVDS Data Port-A Lane-1 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-4<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 8 | LA1P_D5 | LVDS Data Port-A Lane-1 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-5<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 9 | LA2N_D6 | LVDS Data Port-A Lane-2 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-6<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 10 | LA2P_D7 | LVDS Data Port-A Lane-2 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-7<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 11 | LACN_D8 | LVDS Data Port-A Lane-C Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-8<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 12 | LACP_D9 | LVDS Data Port-A Lane-C Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-9<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |

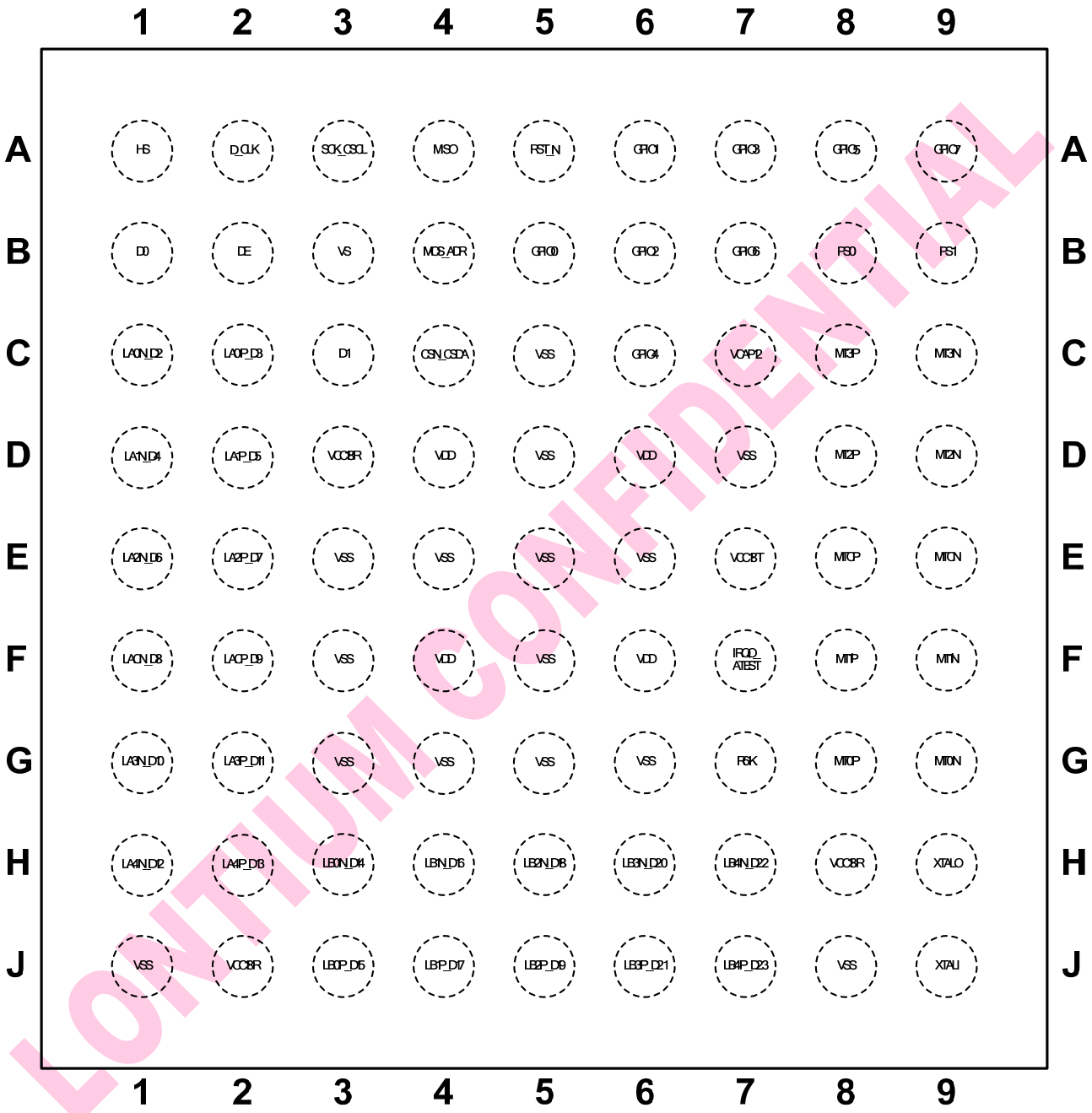
| Pin No. | Pin Name | Pin Description |
|---|---|---|
| 13 | LA3N_D10 | LVDS Data Port-A Lane-3 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-10<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 14 | LA3P_D11 | LVDS Data Port-A Lane-3 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-11<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 15 | LA4N_D12 | LVDS Data Port-A Lane-4 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-12<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 16 | LA4P_D13 | LVDS Data Port-A Lane-4 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-13<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 17 | VCC18R | Analog 1.8V Power<br>1.8V power for RXPLL |
| 18 | LB0N_D14 | LVDS Data Port-B Lane-0 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-14<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 19 | LB0P_D15 | LVDS Data Port-B Lane-0 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-15<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 20 | LB1N_D16 | LVDS Data Port-B Lane-1 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-16<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 21 | LB1P_D17 | LVDS Data Port-B Lane-1 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-17<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 22 | LB2N_D18 | LVDS Data Port-B Lane-2 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-18<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 23 | LB2P_D19 | LVDS Data Port-B Lane-2 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-19<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |

| Pin No. | Pin Name | Pin Description |
|---|---|---|
| 24 | LB3N_D20 | LVDS Data Port-B Lane-3 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-20<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 25 | LB3P_D21 | LVDS Data Port-B Lane-3 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-21<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 26 | LB4N_D22 | LVDS Data Port-B Lane-4 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-22<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 27 | LB4P_D23 | LVDS Data Port-B Lane-4 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-23<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| 28 | VCC18R | Analog 1.8V Power<br>1.8V power for LVDS Receiver Port-2 and Bandgap |
| 29 | R6K | BandGap External Resistor<br>External 6K resistor for setting internal reference current. |
| 30 | IRQO_ATEST | Interrupt Request Output<br>In default, this pin is configured as interrupt request (IRQ) output.<br>Analog Test Signal Output<br>When this pin is configured as Hi-Z, it serves as analog test signal output. |
| 31 | XTALI | Crystal Clock Input<br>A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT8918 |
| 32 | XTALO | Crystal Clock Output<br>A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating. |
| 33 | VCC18T | Analog 1.8V Power<br>1.8V power for MIPI Transmitter |
| 34 | MT0P | MIPI® Data Lane-0 Positive Output<br>MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 35 | MT0N | MIPI® Data Lane-0 Negative Output<br>MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 36 | MT1P | MIPI® Data Lane-1 Positive Output<br>MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 37 | MT1N | MIPI® Data Lane-1 Negative Output<br>MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 38 | MTCP | MIPI® Data Lane-C Positive Output<br>MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |

| Pin No. | Pin Name | Pin Description |
|---|---|---|
| 39 | MTCN | MIPI® Data Lane-C Negative Output<br>MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 40 | MT2P | MIPI® Data Lane-2 Positive Output<br>MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 41 | MT2N | MIPI® Data Lane-2 Negative Output<br>MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 42 | MT3P | MIPI® Data Lane-3 Positive Output<br>MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 43 | MT3N | MIPI® Data Lane-3 Negative Output<br>MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s. |
| 44 | VCAP12 | Internal 1.8V-to-1.2V LDO output<br>Connect this pin to a bypass capacitor no less than 1uF. When configured as using internal bypass capacitor, please put this pin floating. |
| 45 | PS1 | SPI Mode Select Input Bit-1<br>SPI mode select input bit-1. |
| 46 | PS0 | SPI Mode Select Input Bit-0<br>SPI mode select input bit-0. |
| 47 | GPIO7 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| 48 | GPIO6 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| 49 | GPIO5 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| 50 | GPIO4 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| 51 | GPIO3 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| 52 | GPIO2 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| 53 | GPIO1 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| 54 | GPIO0 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| 55 | VDD | Digital core 1.8V Power<br>1.8V power for digital core |

| Pin No. | Pin Name | Pin Description |
|---|---|---|
| 56 | RST_N | Hardware Reset Input<br>Chip reset signal. Active LOW. |
| 57 | MISO | SPI Slave Serial Data Output<br>It serves as the serial port data output for SPI slave register access. |
| 58 | MOSI_ADR | SPI Slave Serial Data Input<br>It serves as the serial port data input for SPI slave register access.<br>I2C Device Address Select<br>It serves as the serial port address select for I2C slave register access. |
| 59 | VDD | Digital core 1.8V Power<br>1.8V power for digital core |
| 60 | SCK_CSCL | SPI Slave Serial Clock Input<br>It serves as the serial port clock input for SPI slave register access.<br>I2C Serial Clock Input<br>It serves as the serial port data clock slave for I2C slave register access. Supports 1.8/3.3V CMOS logic. |
| 61 | CSN_CSDA | SPI Slave Select<br>It serves as the chip select input for SPI slave register access. Active LOW.<br>I2C Serial Data Input/Output<br>It serves as the serial port data IO for I2C slave register access. Supports 1.8/3.3V CMOS logic. |
| 62 | D_CLK | RGB Pixel Clock Input<br>1.8V/3.3V RGB clock GPI input with internal 100K pull-down resistor. |
| 63 | VS | Vertical Sync Input<br>1.8V/3.3V GPI input with internal 100K pull-down resistor. |
| 64 | HS | Horizontal Sync Input<br>1.8V/3.3V GPI input with internal 100K pull-down resistor. |
| 65 | #EPAD | EPAD |

# BGA81 Ball Map



# Ball Definition

| Ball No. | Ball Name | Ball Description |
|---|---|---|
| C5, D5, D7, E3, E4, E5, E6, F3, F5, G3, G4, G5, G6, J1, J8 | VSS | Chip Ground<br>1.8V ground for LT8918 |
| D4, D6, F4, F6 | VDD | Digital core 1.8V Power<br>1.8V power for digital core |
| D3, H8, J2 | VCC18R | Analog 1.8V Power<br>1.8V power for rxphy and rxpll |
| E7 | VCC18T | Analog 1.8V Power<br>1.8V power for mipitx, txpll, and dessc pll |
| C9 | MT3N | MIPI D-PHY Data Lane-3 Negative Input<br>MIPITX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. |
| C8 | MT3P | MIPI D-PHY Data Lane-3 Positive Input<br>MIPITX Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. |
| D9 | MT2N | MIPI D-PHY Data Lane-2 Negative Input<br>MIPITX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. |
| D8 | MT2P | MIPI D-PHY Data Lane-2 Positive Input<br>MIPITX Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. |
| E9 | MTCN | MIPI D-PHY Clock Lane Negative Input<br>MIPITX Negative input of DDR clock differential pairs up to 1.25GHz in quadrature phase with data signals |
| E8 | MTCP | MIPI D-PHY Clock Lane Positive Input<br>MIPITX Positive input of DDR clock differential pairs up to 1.25GHz in quadrature phase with data signals |
| F9 | MT1N | MIPI D-PHY Data Lane-1 Negative Input<br>MIPITX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. |
| F8 | MT1P | MIPI D-PHY Data Lane-1 Positive Input<br>MIPITX Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s. |
| G9 | MT0N | MIPI D-PHY Data Lane-0 Negative Input<br>MIPITX Negative input of Bi-directional polarity swappable differential pairs up to 1.5Gb/s. |
| G8 | MT0P | MIPI D-PHY Data Lane-0 Positive Input<br>MIPITX Positive input of Bi-directional polarity swappable differential pairs up to 1.5Gb/s. |

| Ball No. | Ball Name | Ball Description |
|---|---|---|
| G7 | R6K | BandGap External Resistor<br>External 6K resistor for setting internal reference current. |
| J9 | XTALI | Crystal Clock Input<br>A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT8918. |
| H9 | XTALO | Crystal Clock Output<br>A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating. |
| F7 | IRQO_ATEST | Interrupt Request Output<br>In default, this pin is configured as interrupt request (IRQ) output.<br>Analog Test Signal Output<br>This pin can also be configured as analog debug pin. |
| C7 | VCAP12 | Internal 1.2V LDO Output<br>1.2V LDO output for MIPITX LPTX. Based on configuration, a bypass capacitor might be required to connect to this pin. |
| A2 | D_CLK | RGB Pixel Clock Input<br>1.8V/3.3V RGB clock GPI input with internal 100K pull-down resistor. |
| B3 | VS | Vertical Sync Input<br>1.8V/3.3V GPI input with internal 100K pull-down resistor. |
| A1 | HS | Horizontal Sync Input<br>1.8V/3.3V GPI input with internal 100K pull-down resistor. |
| B2 | DE | RGB Data Active Input<br>1.8V/3.3V GPI input with internal 100K pull-down resistor. |
| B1 | D0 | RGB Data Input Bit-0<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| C3 | D1 | RGB Data Input Bit-1<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| C1 | LA0N_D2 | LVDS Data Lane-0 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-2<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| C2 | LA0P_D3 | LVDS Data Port-A Lane-0 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-3<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| D1 | LA1N_D4 | LVDS Data Port-A Lane-1 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-4<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |

| Ball No. | Ball Name | Ball Description |
|---|---|---|
| D2 | LA1P_D5 | LVDS Data Port-A Lane-1 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-5<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| E1 | LA2N_D6 | LVDS Data Port-A Lane-2 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-6<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| E2 | LA2P_D7 | LVDS Data Port-A Lane-2 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-7<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| F1 | LACN_D8 | LVDS Data Port-A Lane-C Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-8<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| F2 | LACP_D9 | LVDS Data Port-A Lane-C Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-9<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| G1 | LA3N_D10 | LVDS Data Port-A Lane-3 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-10<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| G2 | LA3P_D11 | LVDS Data Port-A Lane-3 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-11<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| H1 | LA4N_D12 | LVDS Data Port-A Lane-4 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-12<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| H2 | LA4P_D13 | LVDS Data Port-A Lane-4 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-13<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| H3 | LB0N_D14 | LVDS Data Port-B Lane-0 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-14<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |

| Ball No. | Ball Name | Ball Description |
|---|---|---|
| J3 | LB0P_D15 | LVDS Data Port-B Lane-0 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-15<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| H4 | LB1N_D16 | LVDS Data Port-B Lane-1 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-16<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| J4 | LB1P_D17 | LVDS Data Port-B Lane-1 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-17<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| H5 | LB2N_D18 | LVDS Data Port-B Lane-2 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-18<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| J5 | LB2P_D19 | LVDS Data Port-B Lane-2 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-19<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| H6 | LB3N_D20 | LVDS Data Port-B Lane-3 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-20<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| J6 | LB3P_D21 | LVDS Data Port-B Lane-3 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-21<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| H7 | LB4N_D22 | LVDS Data Port-B Lane-4 Negative Input<br>LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-22<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| J7 | LB4P_D23 | LVDS Data Port-B Lane-4 Positive Input<br>LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.<br>RGB Data Input Bit-23<br>1.8V/3.3V RGB data GPI input with internal 100K pull-down resistor. |
| B9 | PS1 | SPI Mode Select Input Bit-1<br>SPI mode select input bit-1. |
| B8 | PS0 | SPI Mode Select Input Bit-0<br>SPI mode select input bit-0. |
| A9 | GPIO7 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |

| Ball No. | Ball Name | Ball Description |
|---|---|---|
| B7 | GPIO6 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| A8 | GPIO5 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| C6 | GPIO4 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| A7 | GPIO3 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| B6 | GPIO2 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| A6 | GPIO1 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| B5 | GPIO0 | Digital Test Signal Output<br>GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin. |
| A5 | RST_N | Hardware Reset Input<br>Chip reset signal. Active LOW. |
| A4 | MISO | SPI Slave Serial Data Output<br>It serves as the serial port data output for SPI slave register access. |
| B4 | MOSI_ADR | SPI Slave Serial Data Input<br>It serves as the serial port data input for SPI slave register access.<br>I2C Device Address Select<br>It serves as the serial port address select for I2C slave register access. |
| A3 | SCK_CSCL | SPI Slave Serial Clock Input<br>It serves as the serial port clock input for SPI slave register access.<br>I2C Serial Clock Input<br>It serves as the serial port data clock slave for I2C slave register access. Supports 1.8/3.3V CMOS logic. |
| C4 | CSN_CSDA | SPI Slave Select<br>It serves as the chip select input for SPI slave register access. Active LOW.<br>I2C Serial Data Input/Output<br>It serves as the serial port data IO for I2C slave register access. Supports 1.8/3.3V CMOS logic. |

# Ordering Information

| Part Number | Operating Temperature Range | Package | Packing Method |
|---|---|---|---|
| LT8918 | -40°C to 85°C | 7.5mm x 7.5mm QFN64 | Tape and Reel |

## Lontium Semiconductor Proprietary & Confidential



Visit our corporate web page at: www.lontiumsemi.com
Technical support: support@lontium.com
Sales: sales@lontium.com