DATA SHEET

NVIDIA Jetson AGX Xavier Series System-on-Module

Volta GPU + Carmel CPU + LPDDR4x + eMMC

NVIDIA Jetson AGX Xavier Modules:

JAX: Volta GPU + Carmel CPU + 32 GB LPDDR4x + 32 GB eMMc

JAXi: Volta GPU + Carmel CPU + 32 GB LPDDR4x (ECC support) + 64 GB eMMC + 64 MB NOR

References to JAX include (can be read as) JAXi except where explicitly noted.

Volta GPU

Tensor Cores | End-to-end lossless compression | Tile Caching | OpenGL® 4.6 | OpenGL ES 3.2 | Vulkan™ 1.0 | CUDA® 10

Carmel CPU Complex

ARMv8.2 (64-bit) heterogeneous multi-processing (HMP) CPU architecture | dual-core CPU clusters connected by a high-performance system coherency interconnect fabric | L3 Cache: 4MB (shared across all clusters)

NVIDIA Carmel (Dual-Core) Processor: L1 Cache: 128KB L1 instruction cache (I-cache) per core; 64KB L1 data cache (D-cache) per core | L2 Unified Cache: 2MB per cluster

Audio Subsystem

Dedicated programmable audio processor | ARM Cortex A9 with NEON | I2S outputs: 4x (JAX), **3x (JAXi)** | 2 x I and Q baseband data channels | PDM in/out | Industry-standard High Definition Audio (HDA) controller provides a multi-channel audio path to the HDMI interface.

Memory

256-bit DRAM interface | Secure External Memory Access Using TrustZone Technology | System MMU | **ECC (enabled by software for JAXi only)** | Memory Type: LPDDR4x | Memory Size: 32GB

Storage

eMMC 5.1 Flash Storage | Bus Width: 8-bit | Maximum Bus Frequency: 200MHz (HS400) | Storage Capacity: 32GB (JAX); **64GB (JAXi)**

QSPI NOR Flash Storage **(JAXi Only)** | Bus Width: 32-bit | Maximum Bus Frequency: 65MHz | Storage Capacity: **64MB (JAXi)**

Networking

10/100/1000 BASE-T Ethernet | Media Access Controller (MAC) | RGMII Interface

Imaging

16 lanes (supporting up to 4x4, 6x2, 6x1 configurations) | MIPI CSI-2 | D-PHY 1.2 (up to 2.5Gb/s per lane, total bandwidth up to 40 Gbps) | C-PHY 1.1 (1.7Gsym/s per trio, total bandwidth up to 62 Gbps)

Display Controller Subsystem

Three multi-mode (eDP/DP/HDMI) Serial Output Resources (SOR) | HDMI 2.0a/b (up to 6Gbps), DP 1.4, eDP 1.4 (up to 5.4Gbps) | HDCP 1.4 and 2.2.

Maximum Resolution (DP/eDP/HDMI): (up to) 3840x2160 at 60Hz (up to 36 bpp)

Multi-Stream HD Video & JPEG

Video Encode: H.265 (HEVC), H.264, VP9

Video Decode: H.265 (HEVC), H.264, VP9, VP8, MPEG-4, MPEG-2, VC-1

JPEG (Decode & Encode)

Peripherial Interfaces

USB: xHCI host controller with integrated PHY (up to) 3 x USB 3.1, 4 x USB 2.0; USB 3.0 device controller with integrated PHY | PCIe: x8, x4, x2, (2x) x1 | SD/MMC controller (supporting eMMC 5.1, SD 4.0, SDHOST 4.0 and SDIO 3.0) | 5x UART | 3 x SPI | 5 x I2C | 2 x CAN | GPIOs.

Mechanical

Module Size: 100 mm x 87 mm | PCB: 12L ELIC HDI | Connector: 699 pin B2B connector | Integrated Thermal Transfer Plate (TTP) with Heatpipe.

Operating Requirements

Temperature Range: -25C – 80C (JAX); **-40C – 85C (JAXi)** | Maximum Module Power: 30W (JAX); **40W (JAXi)** | Power Input: System Voltage Input 9.0V – 20.0V; 5V Input: 5.0V | Operating Lifetime (24x7): 5 years (JAX); **10 years (JAXi)**

Refer to the documentation provided with each software release for additional information on current software support.

Revision History

Version	Date	Description
1.3	November 25, 2020	Initial release including information for Jetson AGX Xavier Industrial.
1.4	January 12, 2021	Introduced JAX and JAXi abbreviations for Jetson AGX Xavier and Jetson AGX Xavier Industrial, respectively. Memory Subsystem: Corrected LPDDR4x Memory Bus Table. Table incorrectly listed a 64GB memory size for JAXi. This was corrected to 32GB
1.5	June 11, 2021	Description • Audio Subsystem: updated number of I2S outputs for JAXi • Memory: updated to include ECC support for JAXi • Imaging: added description of CSI interface • Peripherial Interfaces: updated number of UART interfaces for JAXi • Operating Requirements: updated to include Operating Lifetime, updated Temperature Range and Maximum Module Power for JAXi Functional Description • Added Programmable Computer-Vision Accelerator (PVA) description • Added Safety Cluster Engine (SCE) description Volta GPU: Updated JAXi GPU operating frequency Carmel CPU Complex: Updated JAXi CPU operating frequency Memory Subsystem: Updated to include ECC support for JAXi High Definition (HD) Audio/Video Subsystem • Multi-Standard Video Decoder: updated Supported Video Decoder Standards for JAXi • Multi-Standard Video Encoder: updated Supported Video Encoder Standards for JAXi Power and System Management • VCC_RTC: updated to include current draw for backup cell • Power Sequencing: removed Power Sequencing Diagrams, Refer to the *Jetson AGX Xavier Series Module Product Design Guide* for this information. Absolute Maximum Ratings: Updated Max Operating and Storage temperatures for JAXi Environmental & Mechanical Screening: Updated JAXi Testing table to include MTBF information Package Drawing and Dimensions: Updated Module Outline Drawing Module Marking: Updated Module Marking for JAXi

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1 Functional Description

The Jetson AGX Xavier (JAX) series module is a high performance, small-form factor device. It enables modular system design by mechanically isolating integrated components from external mechanical forces, standardizing thermal and mechanical interfaces, and exposing a comprehensive set of system and peripheral interfaces at the 699-pin board-to-board connector. JAX series module can be used in a wide variety of applications requiring varying performance metrics. To accommodate these varying conditions, JAX series modules implement a multi-tiered solution that focuses on the efficient application of performance as a means to manage a complex environment:

- **Power Management Controller (PMC)**: The PMC primarily controls voltage transitions for the Xavier SoC as it transitions to/from different low power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake event from dedicated GPIO which can wake the module from a deep sleep state.
- **Power Gating**: JAX series modules aggressively employ power-gating (controlled by the PMC) to power-off blocks which are idle. CPU cores are on a separate power rail to allow complete removal of power and eliminate leakage. Each CPU can be power gated independently internally. Software provides context save/restore to/from DRAM.
- **Clock Gating**: Used to further reduce unnecessary power consumption where power gating is not an option.
- **Dynamic Voltage and Frequency Scaling (DVFS)**: Raises voltages and clock frequencies when demand requires, Lowers them when less is sufficient, and removes them when none is needed. DVFS is used to change the voltage and frequencies on the following rails: VDD_CPU0, VDD_CPU1, VDD_GPU, and VDD_CV.
- **Real Time Clock (RTC)**: The RTC Always On partition logic of the CPU Complex is not power gated and can wake the system based on either a timer event or an external trigger (e.g., key press).

JAX series modules have two power inputs: 1) a 5V Regulator input and 2) a 9V - 20V input. Power is then supplied to the devices on board through a power management IC (PMIC) and dedicated voltage regulators; all internal module voltages and IO voltages are generated from this input. An optional back up battery can be attached to the VCC_RTC module input (this will maintain the on system RTC, when VIN is not present). VIN must be supplied by the carrier board that the JAX module is designed to connect to.

1.1 Volta GPU

The same Volta GPU architecture that powers NVIDIA high-performance computing (HPC) products was adapted for use in JAX series modules. The Volta architecture features a new Streaming Multiprocessor (SM) optimized for deep learning. The new Volta SM is far more energy efficient than the previous generations enabling major performance boosts in the same power envelope. The Volta SM includes:

- New programmable Tensor Cores purpose-built for INT8/FP16/FP32 deep learning tensor operations; IMMA and HMMA instructions accelerate integer and mixed-precision matrix-multiply-and-accumulate operations.
- Enhanced L1 data cache for higher performance and lower latency.
- Streamlined instruction set for simpler decoding and reduced instruction latencies.
- Higher clocks and higher power efficiency.

The Volta architecture also incorporates a new generation of its memory subsystem and enhanced unified memory and address translation services that increases memory bandwidth and improves utilization for greater efficiency.

The Graphics Processing Cluster (GPC) is a dedicated hardware block for compute, rasterization, shading, and texturing; most of the GPU's core graphics functions are performed inside the GPC. It is comprised of Texture Processing Clusters (TPC), with each TPC containing two SM units, and a Raster Engine. The SM unit creates, manages, schedules and executes instructions from many threads in parallel. Raster operators (ROPs) continue to be aligned with L2 cache slices and memory controllers. The SM geometry and pixel processing performance make it highly suitable for rendering advanced user interfaces; the efficiency of the Volta GPU enables this performance on devices with power-limited environments.

Each SM is partitioned into four separate processing blocks (referred to as SMPs), each SMP contains its own instruction buffer, scheduler, CUDA cores and Tensor cores. Inside each SMP, CUDA cores perform pixel/vertex/geometry shading and physics/compute calculations, and each Tensor core provides a 4x4x4 matrix processing array to perform mixed-

precision fused multiply-add (FMA) mathematical operations. Texture units perform texture filtering and load/store units fetch and save data to memory. Special Function Units (SFUs) handle transcendental and graphics interpolation instructions. Finally, the PolyMorph Engine handles vertex fetch, tessellation, viewport transform, attribute setup, and stream output.

Table 1 GPU Operation

Module	GPC Configuration			Performance (peak)	Operating Frequency per Core (up to)
	Number of TPC	CUDA Cores	Tensor Cores		
JAX	4	512	64	10 TFLOPS | 32 TOPS	1.37 GHz
JAXi	**4**	**512**	**64**	**10 TFLOPS | 30 TOPS**	**1.21 GHz**

Features:

- End-to-end lossless compression
- Tile Caching
- OpenGL 4.6, OpenGL ES 3.2, and Vulkan 1.0

  Product is based on a published Khronos Specification and is expected to pass the Khronos Conformance Process. Current conformance status can be found at www.khronos.org/conformance.

- Adaptive Scalable Texture Compression (ATSC) LDR profile supported
- DirectX 12 compliant
- CUDA support
- Iterated blend, ROP OpenGL-ES blend modes
- 2D BLIT from 3D class avoids channel switch
- 2D color compression
- Constant color render SM bypass
- 2x, 4x, 8x MSAA with color and Z compression
- Non-power-of-2 and 3D textures, FP16 texture filtering
- FP16 shader support
- Geometry and Vertex attribute Instancing
- Parallel pixel processing
- Early-z reject: Fast rejection of occluded pixels acts as multiplier on pixel shader and texture performance while saving power and bandwidth
- Video protection region
- Power saving: Multiple levels of clock gating for linear scaling of power

1.2 Carmel CPU Complex

The CPU complex (CCPLEX) is comprised of Carmel dual-core CPU clusters in a coherent multi-processor configuration. A high-performance System Coherency Fabric (SCF) connects all CPU clusters enabling simultaneous operation of all CPU cores (as needed) for a true heterogeneous multi-processing (HMP) environment.

The SCF also connects CPU clusters to:

- DRAM through the Memory Controller Fabric (MCF).
- Other processing and I/O blocks in the Memory Mapped I/O (MMIO) space through an ARM Advanced eXtensible Interface (AXI).

Each CPU cluster contains two identical Carmel processors; each core includes 128 KB Instruction (I-cache) and 64 KB Data (D-cache) Level 1 caches, a 2 MB L2 cache is shared by both cores.

Table 2 CPU Operation

Module	CPU Configuration			CPU Cores	Operating Frequency per Core (up to) *
	CPU Cluster	L2 Cache	L3 Cache		
JAX	4 x dual-core	8MB	4MB	8	2.26Ghz
JAXi	**4 x dual-core**	**8MB**	**4MB**	**8**	**2.03GHz**

* Refer to the documentation provided with each software release for additional information on supported power modes and CPU operation.

Features:

- NVIDIA Dynamic Code Optimization
- 10-wide Superscalar architecture
- Dynamic branch prediction with a Branch Target Buffer and Global History Buffer RAMs, a return stack buffer, and an indirect predictor.
- Full implementation of ARMv8.2 ISA compliant architecture including:
    - ARMv8 TrustZone
    - ARMv8.0 Crypto ISA
    - Trusted Memory
        - TZ-RAM
        - TZ-DRAM
        - Dynamic CMA VPR
        - GSC DRAM Carveouts
        - Clock Monitoring
        - Voltage Monitoring
        - Trusted Boot
        - Trusted Debug
    - ARMv8.2-FP16 support
- 128 KB 4-way-associative parity protected L1 instruction cache per core
- 64 KB 4-way-associative parity protected L1 data cache per core
- 2 MB 16-way-associative ECC protected L2 cache per CPU cluster
- 4 MB 16-way-associative ECC protected L3 cache (shared across all clusters)
- Performance Monitoring
- Interface to an external Generic Interrupt Controller (vGIC-400)
- Support for power management with multiple power domains

1.3 Memory Subsystem

The Memory Subsystem (MSS) provides access to local DRAM, SysRAM, and provides a SyncPoint Interface for inter-processor signaling. The memory subsystem supports full-speed I/O coherence by routing requests through a scalable coherence fabric. It also supports a comprehensive set of safety and security mechanisms.

Structurally, the MSS consists of:

1. MSS Data Backbone - routes requests from clients to the MSS Hub and responses from MSS Hub to the clients.
2. MSS Hub - receives and arbitrates among client requests, performs SMMU translation, and sends requests to the MCF.
3. Memory Controller Fabric (MCF) - performs security checks, feeds I/O coherent requests to the Scalable Coherence Fabric (SCF), and directs requests to the multiple memory channels.
4. Memory Controller (MC) Channels - row sorter/arbiter and DRAM controllers.
5. DRAM IO - channel-to-pad fabric, DRAM I/O pads, and PLLs.

JAX series modules integrate a 256-bit wide LPDDR4X memory interface implemented as eight 32-bit channels with x16 sub-partitions. The memory controller provides a single read or write command and row address to both sub-partitions in the channel to transfer 64 bytes, but provides three independent column address bits to each sub-partition, allowing it access different 32 byte sectors of a GOB between the sub-partitions. It provides connections between a wide variety of clients, supporting their bandwidth, latency, quality-of-service needs and any special ordering requirements that are needed. The MSS supports a variety of security and safety features and address translation for clients that use virtual addresses.

Table 3 LPDDR4x Memory Bus

Module	Size	Maximum Bandwidth	Maximum Bus Frequency	ECC Support
JAX	32GB	136.5GB/s	2133MHz	No
JAXi	**32GB**	**136.5GB/s**	**2133MHz**	**Yes (enabled by software)**

Features:

- LPDDR4X: x32 DRAM chips
- 256-bit wide data bus
- Low Latency Path and Fast Read/Response Path Support for the CPU Complex Cluster
- Support for low-power modes:
  - Software controllable entry/exit from: self-refresh, power down, deep power down
  - Hardware dynamic entry/exit from: power down, self-refresh
  - Pads use DPD-mode during idle periods
- High-bandwidth interface to the integrated Volta GPU
- Full-speed IO coherence with bypass for Isochronous (ISO) traffic
- System Memory-Management Unit (SMMU) for address translation based on the ARM SMMU-500
- High-bandwidth PCIe ordered writes
- AES-XTS encryption with 128-bit key
- DRAM ECC **(Enabled by software for JAXi only)**
  - SEC (Single Error Correction)
  - DED (Double Error Detection)
  - Parity protection support

1.4 Video Input

JAX series modules incorporate support for both the MIPI Camera Serial Interface (CSI) and Sony's Scalable Low Voltage Signaling with Embedded Clock (SLVS-EC) interface. Both interfaces work with the Video Input (VI) block to capture an image from a sensor, where NVCSI/SLVS-EC are sources of pixel data to VI. Image capture interfaces work in streaming mode while VI captures the required frames using a single-shot mode of operation. All sync point generation for software is handled at VI; the delay between image capture and VI is negligible in software terms. Image capture interfaces do not have a direct memory port, instead they send the pixel data to memory through VI.

Camera data input interfaces supported: CSI-2 and SLVS-EC v1.2; pixels are already decoded and aligned by the external CSI or SLVS-EC units.

SLVS-EC not supported on JAXi modules

1.4.1 MIPI Camera Serial Interface (CSI)

Standard	Notes
MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), version 2.0, MIPI Alliance, Inc.	Not Supported: • Camera Controller Interface (CCI) • Predictor2
MIPI Alliance Specification for C-PHY, version 1.1, MIPI Alliance, Inc.	
MIPI Alliance Specification for D-PHY, version 1.2, MIPI Alliance, Inc.	

Fifth-generation NVIDIA camera solution (NVCSI 2.0, VI 5.0, and ISP 5.0) provides a combination host that supports both MIPI C-PHY and enhanced MIPI D-PHY (with lane deskew support) physical layer options in four 4-lane, six 2-lane, or six 1-lane configurations; or combinations of these. Each lane can support up to 16 virtual channels (VC) and supports data type interleaving.

- Virtual Channel Interleaving: VCs are defined in the CSI-2 specification and are useful when supporting multiple camera sensors. With the VC capability, a one-pixel parser (PP) can de-interleave up to 16 image streams.
- Data Type Interleaving: In HDR line-by-line mode, the sensor can output long/short exposure lines using the same VC and a different programmable data type (DT).
- Frequency Target: The parallel pixel processing rate, measured in pixels-per-clock (PPC), is increased to allow higher throughput and lower clock speeds. To support higher bandwidth without increasing the operating frequency, the host processes multiple pixels in one clock. NVCSI is capable of processing four PPCs when bits-per-pixel (BPP) is greater than 16, and eight PPC when BPP is less than or equal to 16.
- With the new streaming mode in NVCSI, one PP can handle all traffic (embedded data and image data) from one camera device, including 16 VCs.

Features:

- Supports both the MIPI D-PHY v1.2 and the MIPI C-PHY v1.1 physical layer options.
  - MIPI D-PHY supports up to 2.5 Gbits/sec per pair, for an aggregate bandwidth of 40 Gbps from 16 pairs
  - MIPI C-PHY supports up to 1.7 G symbol/sec (Gsym/s) per trio
- Based on MIPI CSI-2 v2.0 protocol stack
- Includes six pixel parsers (PP)
- Supports up to 16 virtual channels (VC) per active PP

- Supported input data formats:
  - RGB: RGB888, RGB666, RGB565, RGB555, RGB444
  - YUV: YUV422-8b, YUV420-8b (legacy), YUV420-8b, YUV444-8b
  - RAW: RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20
  - DPCM (predictor 1): 14-10-14, 14-8-14, 12-8-12, 12-7-12, 12-6-12, 12-10-12, 10-8-10, 10-7-10, 10-6-10
- Data type interleave support

1.4.2 Scalable Low Voltage Signaling with Embedded Clock (SLVS-EC) - (JAX only)

Not supported on JAXi modules

Standard	Notes
Scalable Low Voltage Signaling with Embedded Clock (SLVS-EC) Specification v1.2	

SLVS-EC sensors operating in slave mode require the JAX series module to send out a vertical sync signal (XVS) and horizontal sync signal (XHS). The on-board SLVS-EC timing generator (i.e., VI sync generator – SYNCGEN) produces these signals using a fractional-rate divider and drives them to the sensor.

Features:

- Sensor slave mode, shared clock
- Up to 8 lanes
- Up to 2 streams
- Mode change with standby
- 1152 Mbps and 2304 Mbps baud rate
- Supported input data formats:
  - RAW8, RAW10, RAW12, RAW14, RAW16 formats
- Packet footer CRC
- 2 data ID

1.4.3 Video Input (VI) Block

The Video Input (VI) block receives data from the CSI receiver and prepares it for presentation to system memory or the dedicated image signal processor (ISP) execution resources. The VI block provides formatting for RGB, YCbCr, and raw Bayer data in support of a number of camera user models. These models include single and multi-camera systems, which may have up to six active streams. The input streams are obtained from MIPI compliant CMOS sensor camera modules.

1.4.4 Image Signal Processor

The Image Signal Processor (ISP) takes data from the VI or CSI block in raw Bayer format and processes it to YUV output. Advanced image processing is used to convert input to YUV data, and remove artifacts introduced by high-megapixel CMOS sensors, camera lens, and color-space conversion.

Features:

- CSI Virtual Channel (VC) supports four VCs per CSI x4 brick
- Local Tone Map
- Bayer Histogram statistics for auto-exposure
- Bayer average map for auto white balance and auto-exposure
- Sharpness map for auto focus

- Parity Protection
- Bad pixel count
- Deadlock detection

1.5 Display Controller

The JAX series module integrates a unified display controller (based on the NVIDIA NVDisplay architecture) and three independent display outputs. The Display Controller includes a Pixel Processing Engine that fetches pixel data to be processed from DRAM and generates up to six windows of rasterized display-ready pixel data. The instructions for processing the pixel data are captured by the display controller's Front End (FE) logic, which then generates the individual controls for the various stages of pixel processing. The pixel data to be processed are fetched in the Isochronous Memory Hub (IsoHub) then go through the specified pixel processing, including merging the cursor, in four pipe stages: Pre-Composition (Pre-comp); Composition (Comp); Post-Composition (Post-comp); and Raster Generation (RG). The rasterized display-ready pixel data are available for the separate panels/devices (referred to as display heads) and are fed through a multi-channel crossbar structure to the Serial Output Resources (SOR) in the Display Interface for the standard display output format, i.e. DP (Display Port) and HDMI (High Definition Multimedia Interface).

Each of the display heads can be run at an independent clock rate, and each can drive a different display resolution. Each of the six display windows (A, B, C, D, E, F) can be arbitrarily assigned to any of the display Heads as required, then connected to any one of the display heads for desired output format.

Features:

- Integrated HDCP key storage, no external SecureROM required
- Six windows that can be assigned to any Head
- One special-purpose TrustZone® protected window on Head0
- Maximum raster size: 32768 x 32768
- Maximum active region: 8192 x 8192
- Maximum input surface size: 32768 x 32768
- Maximum fetched size: 8192 x 8192
- Input surface color formats:
    - 16-bit RGB: R4G4B4A4, R5G6B5, A1R5G5B5, and R5G5B5A1
    - 24-bit RGB: A8R8G8B8, X8R8G8B8, A8B8G8R8, and X8B8G8R8
    - 32-bit RGB: A2R10G10B10, A2B10G10R10, X2BL10GL10RL10_XRBIAS, and X2BL10GL10RL10_XVYCC
    - 64-bit RGB: R16_G16_B16_A16_NVBIAS, and R16_G16_B16_A16
    - Packed YUV 422: Y8_U8_Y8_V8_N422, and U8_Y8_V8_Y8_N422
    - Semi Planar YUV 422 (8, 10, 12 bpc):
        - Y8_V8U8_N422, Y8_V8U8_N422R
        - Y10_V10U10_N422, Y10_V10U10_N422R
        - Y12_V12U12_N422, Y12_V12U12_N422R
    - Semi-planar YUV 420 (8, 10, 12 bpc):
        - Y8_V8U8_N420*
        - Y10_V10U10_N420*
        - Y12_V12U12_N420*
    - Semi-planar YUV 444 (8 ,10, 12 bpc):
        - Y8_V8U8_N444
        - Y10_V10U10_N444
        - Y12_V12U12_N444
    - Planar YUV 420 (8, 10, 12 bpc):
        - Y8_U8_V8_N420
        - Y10_U10_V10_N420
        - Y12_U12_V12_N420

    - Planar YUV 444 (8, 10, 12 bpc):
        - Y8_U8_V8_N444
        - Y10_U10_V10_N444
        - Y12_U12_V12_N444
- Pipeline depth
    - 16-bpc, [-1.5, 2.5] range (two range extension bits): De-gamma will clip to 0,1 immediately on the input
- Vsync (VCOUNTER) and immediate (HCOUNTER) flip modes
    - Immediate flip supported for RGB only
    - Immediate flips occur at the second 8-line boundary after the current line.

- Cursor cannot be enabled on a Head unless the Head has at least one window group attached. The window group does not need to be enabled.
- TrustZone cannot be enabled unless Head0 has at least one window group attached. This does not need to be enabled.
- Color formats marked with an asterisk (*) are programmed as Y_UV in the display manuals, and then byte-swapped later to be Y_VU.
- 10-bpc and 12-bpc YUV color formats are packed into 16-bpc containers. This effectively limits immediate flips to no faster than one every 16 lines.

1.5.1 High-Definition Multimedia Interface (HDMI) and DisplayPort (DP) Interfaces

Standard	Notes
High-Definition Multimedia Interface (HDMI) Specification, version 2.0a/b	> 340 MHz pixel clock Scrambling support Clock/4 support (1/40 bit-rate clock)
VESA DisplayPort Standard Version 1.4	
HDMI® Specification 2.0	HDMI 1.4 (up to 340 MHz pixel clock rate) HDMI 2.0 (up to 594 MHz pixel clock rate)

A standard DP 1.4 or HDMI 2.0a/b interface is supported. These share the same set of interface pins, so either DisplayPort or HDMI can be supported natively. Dual-Mode DisplayPort (DP++) can be supported, in which the DisplayPort connector logically outputs TMDS signaling to a DP-to-HDMI dongle. Each output collects the output of a display pipeline from the display controller, formats/encodes that output (to a desired format), and then streams it to an output device. Each output is capable of providing an interface to an external device; each output can drive only a single output device at any given time. HDMI support provides a method of transferring both audio and video data; the SOR receives video from the display controller and audio from a separate high-definition audio (HDA) controller, it combines and transmits them as appropriate.

A single CEC controller is shared between HDMI and DP interfaces and can only be applied for use on one interface (i.e., does not support multiple instances if both interfaces were used for HDMI).

Features:

- DisplayPort
    - (up to) 540MHz pixel clock rate (i.e., 1.62GHz for RBR, 2.7GHz for HBR, and 5.4GHz for HBR2).
    - 8b/10b encoding support
    - External Dual Mode standard support

    - Audio streaming support
- HDMI
    - (up to) 594 MHz pixel clock
        - 8/12 bpc RGB and YUV444
        - 8/10/12 bpc YUV422
        - 8 bpc YUV420 (10/12 bpc YUV frame buffers should be output as YUV422)
    - HDMI Vendor-Specific Infoframe (VSI) packet transmission
    - On HDMI, multichannel audio from HDA controller, up to 8 channels, 192 KHz, 24-bit.
    - Fuse calibration information for HDMI analog parameter(s)
    - 1080i output on HDMI
- DP or HDMI connectors via appropriate external level shifting
- HDCP 2.2 and 1.4 over either DP or HDMI
- External Dual Mode standard (DP2HDMI passive or active adapters and adapter discovery)
- Generic infoframe transmission
- Frame-packed 3D stereo mode
- Safety based on Register Parity

* (Resolution + Refresh Rate + Pixel Depth + Format) must be within specification limits to achieve support for desired pixel depth.

1.5.2 Embedded DisplayPort (eDP) Interface

Standard	Notes
VESA Embedded DisplayPort Standard Version 1.4	

eDP is a mixed-signal interface consisting of four differential serial output lanes and one PLL. This PLL is used to generate a high frequency bit-clock from an input pixel clock enabling the ability to handle 10-bit parallel data per lane at the pixel rate for the desired mode. Embedded DisplayPort (eDP) modes (1.6 GHz for RBR; 2.16 GHz, 2.43 GHz, and 2.7 GHz for HBR; 3.24 GHz, 4.32 GHz, and 5.4 GHz for HBR2).

eDP has been tested according to DP1.2b PHY CTS even though eDPv1.4 supports lower swing voltages and additional intermediate bit rates. This means the following nominal voltage levels (400mV, 600mV, 800mV, 1200mV) and data rates (RBR, HBR, HBR2) are tested. This interface can be tuned to drive lower voltage swings below 400mV and can be programmed to other intermediate bit rates as per the requirements of the panel and the system designer.

The eDP block collects pixels from the output of the display pipeline, formats/encodes them to the eDP format, and then streams them to various output devices. It drives local panels only (does not support an external DP port), includes a small test pattern generator and CRC generator.

Features:

- 1/2/4/ lane, single link
- additional link rates (2.16, 2.43, 3.24, 4.32 Gbps)
- enhanced framing
- power sequencing
- reduced auxiliary timing
- reduced main voltage swing
- ASSR (alternate seed scrambler reset) for internal eDP panels

1.6 High Definition (HD) Audio/Video Subsystem

The HD Audio-Video Subsystem uses a collection of functional blocks to off-load audio and video processing activities from the CPU complex, resulting in fast, fully concurrent, highly efficient operation.

This subsystem is comprised of the following:

- (2x) Multi-Standard Video Decoder
- (2x) Multi-Standard Video Encoder
- JPG Processing Block
- Video Image Compositor (VIC)
- Audio Processing Engine (APE)

1.6.1 Multi-Standard Video Encoder

The JAX series module incorporates two instances of the NVIDIA Multi-Standard Video Encoder (NVENC). This multi-standard video encoder enables full hardware acceleration of various encoding standards. It performs high quality video encoding operations for mobile applications such as video recording and video conferencing. The encode processor is designed to be extremely power efficient without sacrificing performance.

Table 4 Supported Video Standards - Encode

Standard	Profile(s)	Module	Resolution (Maximum Number of Streams)	Throughput (up to)
H.265 (HEVC)	Main, Main10	JAX	4K60 (4) | 4K30 (8) | 1080p60 (16) | 1080p30 (32)	(2x) 1000 MP/s
		JAXi	**4K60 (2) | 4K30 (6) | 1080p60 (12) | 1080p30 (24)**	**(2x) 800 MP/s**
	Main 4:4:4, Main 4:4:4 10, MV (per view)	JAX	4K60 (2) | 4K30 (4) | 1080p60 (8) | 1080p30 (16)	(2x) 500 MP/s
		JAXi	**4K30 (12) | 1080p60 (6) | 1080p30 (12)**	**(2x) 400 MP/s**
H.264	Baseline, Main, High	JAX	4K60 (4) | 4K30 (8) | 1080p60 (14) | 1080p30 (30)	(2x) 980 MP/s
		JAXi	**4K60 (2) | 4K30 (6) | 1080p60 (12) | 1080p30 (24)**	**(2x) 790 MP/s**
	High 444, High 444 Predictive, MVC (per view)	JAX	4K60 (2) | 4K30 (4) | 1080p60 (7) | 1080p30 (15)	(2x) 490 MP/s
		JAXi	**4K30 (2) | 1080p60 (6) | 1080p30 (12)**	**(2x) 390 MP/s**
VP9	profile 0	JAX	4K60 (2) | 4K30 (4) | 1080p60 (10) | 1080p30 (20)	(2x) 600 MP/s
		JAXi	**4K60 (1) | 4K30 (2) | 1080p60 (6) | 1080p30 (14)**	**(2x) 480 MP/s**

Bitrate (up to): 15 Mbps for 1080p | 60 Mbps for 2160p
Maximum throughput is half for YUV444 compared to YUV420.
A/V codec, post-processing and containers support are subject to software support; refer to NVIDIA software release notes for detailed specifications. Additional audio codecs may be supported using 3rd parties.

Features:

- Timestamp for Audio/Video Sync
- CBR and VBR rate control (supported in firmware)
- Programmable intra-refresh for error resiliency
- Macro-block based and bit based packetization (multiple slice)
- Motion estimation (ME) only mode

1.6.2 Multi-Standard Video Decoder

The JAX series module incorporates two instances of the NVIDIA Multi-Standard Video Decoder (NVDEC). This video decoder accelerates video decode, supporting low resolution mobile content, Standard Definition (SD), High Definition (HD) and UltraHD (8K, 4K, etc.) video profiles. The video decoder is designed to be extremely power efficient without sacrificing performance. The video decoder communicates with the memory controller through the video DMA which supports a variety of memory format output options. For low power operations, the video decoder can operate at the lowest possible frequency while maintaining real-time decoding using dynamic frequency scaling techniques.

Table 5 Supported Video Standards - Decode

Standard	Profile(s)	Module	Resolution (Maximum Number of Streams)	Throughput (up to)
H.265 (HEVC)	Main, Main10	JAX	8K30 (2) | 4K60 (6) | 4K30 (12) | 1080p60 (26) | 1080p30 (52)	(2x) 1500 MP/s
		JAXi	**8K30 (2) | 4K60 (4) | 4K30 (8) | 1080p60 (18) | 1080p30 (36)**	**(2x) 1200 MP/s**
	Main 4:4:4, Main 4:4:4 10, MVC (per view)	JAX	4K60 (2) | 4K30 (6) | 1080p60 (13) | 1080p30 (26)	(2x) 750 MP/s
		JAXi	**4K60 (2) | 4K30 (4) | 1080p60 (8) | 1080p30 (18)**	**(2x) 600 MP/s**
H.264	Baseline, Main, High	JAX	4K60 (4) | 4K30 (8) | 1080p60 (16) | 1080p30 (32)	(2x) 1000 MP/s
		JAXi	**4K60 (2) | 4K30 (6) | 1080p60 (12) | 1080p30 (24)**	**(2x) 800 MP/s**
	High 444, High 444 Predictive, MVC (per view)	JAX	4K60 (2) | 4K30 (4) | 1080p60 (8) | 1080p30 (16)	(2x) 500 MP/s
		JAXi	**4K30 (2) | 1080p60 (6) | 1080p30 (12)**	**(2x) 400 MP/s**
VP9	profile 0	JAX	4K60 (4) | 4K30 (8) | 1080p60 (19) | 1080p30 (38)	(2x) 1000 MP/s
		JAXi	**4K60 (2) | 4K30 (6) | 1080p60 (12) | 1080p30 (24)**	**(2x) 800 MP/s**

Bitrate (up to): 15 Mbps for 1080p | 60 Mbps for 2160p | 240 Mbps for 4320p
Maximum throughput is half for YUV444 compared to YUV420.
A/V codec, post-processing and containers support are subject to software support; refer to NVIDIA software release notes for detailed specifications. Additional audio codecs may be supported using 3rd parties.

1.6.3 JPEG Processing

The JPEG processing block is responsible for JPEG (de)compression calculations (based on JPEG still image standard), image scaling, decoding (YUV420, YUV422H/V, YUV444, YUV400) and color space conversion (RGB to YUV).

Input (encode) formats:

- Pixel width: 8 bpc
- Subsample format: YUV420
- Resolution (up to): 16K x 16K
- Pixel pack format
    - Semi-planar/Planar for 420

Output (decode) formats:

- Pixel width 8 bpc
- Resolution (up to): 16K x 16K
- Pixel pack format
    - Semi-planar/Planar for YUV420
    - YUY2/Planar for 422H/422V
    - Planar for YUV444/YUV400
    - Interleaved RGBA

1.6.4 Video Image Compositor

The Video Image Compositor (VIC) implements various 2D image and video operations in a power-efficient manner. It handles various system UI scaling, blending, and rotation operations, video post-processing functions needed during video playback, and advanced de-noising functions used for camera capture.

Features:

- Color Decompression
- High-quality De-interlacing
- Inverse Teleciné
- Temporal Noise Reduction
    - New Bilateral Filter as spatial filter
    - Improved TNR3 algorithm
- Scaling
- Color Conversion
- Memory Format Conversion
- Blend/Composite
- 2D Bit BLIT operation
- Rotation
- Geometry transform processing
    - Programmable 9-points controlled warp patch for distortion correction
    - Real-time on-the-fly position generation from sparse warp map surface
    - Pincushion/barrel/moustache distortion correction
    - Distortion correction of 180 and 360 degree wide FOV lens
    - Scene perspective orientation adjustment with IPT
    - Full warp map capability
    - Non-fixed Patch size with 4x4 regions
    - External Mask bit map surface

1.6.5 Audio Processing Engine

The Audio Processing Engine (APE) is a self-contained unit with dedicated audio clocking that enables Ultra Low Power (ULP) audio processing. Software based post processing effects enable the ability to implement custom audio algorithms.

Features:

- 96 KB Audio RAM
- Low latency voice processing
- Audio Hub (AHUB)
  - 4x (JAX), **3x (JAXi)** I2S Stereo/TDM I/O
  - DMIC
  - DSPK
- Multi-Channel IN/OUT
- Digital Audio Mixer: 10-in/5-out
  - Up to eight channels per stream
  - Simultaneous Multi-streams
  - Flexible stream routing
- Multi-band Dynamic Range Compression (DRC)
  - Up to three bands
  - Customizable DRC curve with tunable knee points
  - Up to 192 kHz, 32-bit sample, eight channels
- Parametric equalizer: up to 12 bands
- Low latency sample rate conversion (SRC) and high quality asynchronous sample rate conversion (ASRC)

1.6.5.1 Inter-IC Sound (I2S) Controller

The Inter-IC Sound (I2S) controller implements full-duplex, bidirectional and single direction point-to-point serial interfaces. It can interface with I2S-compatible products, such as compact disc players, digital audio tape devices, digital sound processors, modems, Bluetooth chips, etc. The JAX series module supports I2S audio outputs with I2S/PCM interfaces supporting clock rates up to 24.576 MHz.

Features:

- Basic I2S modes supported (I2S, RJM, LJM, and DSP) in both Initiator and Target modes.
- PCM mode with short (one-bit-clock wide) and long-fsync (two bit-clocks wide) in both Initiator and Target modes.
- Network (Telephony) mode with independent slot-selection for both Tx and Rx
- TDM mode with flexibility in number of slots and slot(s) selection.
- Capability to drive-out a High-z outside the prescribed slot for transmission
- Flow control for the external input/output stream.

Table 6 TDM Timing Parameters (Initiator Mode)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{SCK}	Frequency			24.576	MHz	
T_{CYL}	I2Sx_SCLK cycle time	$1/F_{SCK}$			ns	
T_{FDLY}	I2Sx_LRCK delay	0		4.5	ns	

Symbol	Parameter	Min	Typ	Max	Unit	Notes
t_{DDLY}	I2Sx_SDOUT delay	0		4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	-	-	ns	
t_{DH}	I2Sx_SDIN hold time	2	-	-	ns	
t_{RT}	I2Sx_SCLK rise time			5% * T_{CYL}		
t_{FT}	I2Sx_SCLK fall time			5% * T_{CYL}		
t_{CH}	I2Sx_SCLK high time	45% * T_{CYL}				
t_{CL}	I2Sx_SCLK low time	45% * T_{CYL}				

Table 7 TDM Timing Parameters (Target Mode up to 24.576 MHz)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{SCK}	Frequency			24.576	MHz	
T_{CYL}	I2Sx_SCLK cycle time	$1/F_{SCK}$			ns	
t_{DDLY}	I2Sx_SDOUT delay	0		4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	–	–	ns	
t_{DH}	I2Sx_SDIN hold time	2			ns	
t_{FSU}	I2Sx_LRCK setup	2		45% * T_{CYL} - 2	ns	1
t_{FSH}	I2Sx_LRCK hold	55% T_{CYL} + 2			ns	2
t_{RT}	I2Sx_SCLK rise time			5% * T_{CYL}		
t_{FT}	I2Sx_SCLK fall time			5% * T_{CYL}		
t_{CH}	I2Sx_SCLK high time	45% * T_{CYL}				
t_{CL}	I2Sx_SCLK low time	45% * T_{CYL}				

1. Max t_{FSU} requirement only applies while Fsync Launching on Clock Raising Edge
2. Min t_{FSH} (55% T_{CYL} + 2) requirement only applies while Fsync Launching on Clock Raising Edge; in other use cases, Min t_{FSH} is 2ns.

Table 8 TDM Timing Parameters (Target Mode up to 12.288 MHz)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{SCK}	Frequency			12.288	MHz	
T_{CYL}	I2Sx_SCLK cycle time	1/Fsck			ns	
t_{DDLY}	I2Sx_SDOUT delay	0		4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	–	–	ns	
t_{DH}	I2Sx_SDIN hold time	2			ns	
t_{FSU}	I2Sx_LRCK setup	2		35% * TCYL - 2	ns	1
t_{FSH}	I2Sx_LRCK hold	65% TCYL + 2			ns	2
t_{RT}	I2Sx_SCLK rise time			15%* TCYL		
t_{FT}	I2Sx_SCLK fall time			15%* TCYL		
t_{CH}	I2Sx_SCLK high time	35% * TCYL				
t_{CL}	I2Sx_SCLK low time	35% * TCYL				

1. Max t_{FSU} requirement only applies while Fsync Launching on Clock Raising Edge
2. Min t_{FSH} (35% T_{CYL} + 2) requirement only applies while Fsync Launching on Clock Raising Edge; in other use cases, Min t_{FSH} is 2ns.

1.6.5.2 Digital MIC Controller (DMIC)

The DMIC Controller is used to interface with PDM base input devices. The DMIC controller converts Pulse Density Modulation (PDM) signals to Pulse Code Modulation (PCM) signals.

Features:

- Sample rate support: 8 kHz - 48 kHz
- Input PCM bit width: 16 - 24 bits
- Oversampling Ratio: 64, 128, 256

1.6.5.3 Digital Speaker Controller (DSPK)

The PDM transmit block converts multi-bit PCM audio input to oversampled 1-bit PDM output. The mono or stereo audio is transmitted over a data/clock pair (I^2S interface) to an external codec. The block consists of an interpolator followed by a Delta Sigma Modulator (DSM).

Features:

- Sample rate support: 8 – 48 kHz
- Input PCM bit-width: 16 – 24 bits
- Oversampling Ratio: 64, 128, 256
- Passband frequency response: <= 0.5 dB peak-to-peak in 10 Hz – 20 kHz range
- THD+N: <= -80 dB @ -10 dBFS
- Dynamic Range: >= 105 dB

1.6.6 High Definition Audio (HDA)

Standard
Intel High Definition Audio Specification Revision 1.0a

The JAX series module implements an industry-standard High Definition Audio (HDA) controller. This controller provides a multi-channel audio path to the HDMI interface. The HDA block provides an HDA-compliant serial interface to an audio codec. Multiple input and output streams are supported.

Features:

- Supports HDMI 1.3a and DP1.1
- Support up to four audio streams for use with HDMI/DP
- Supports striping of audio out across 1,2,4[a] SDO lines
- Supports DVFS with maximum latency up to 208 µs for eight channel
- Supports four internal audio codecs
- Audio Format Support
    - Uncompressed Audio (LPCM): 16/20/24 bits at 32/44.1/48/88.2/96/176.4/192[b] kHz
    - Compressed Audio format: AC3, DTS5.1, MPEG1, MPEG2, MP3, DD+, MPEG2/4 AAC, TrueHD, DTS-HD

[a] Four SDO lines: cannot support one stream, 48 kHz, 16-bits, 2 channels; for this case, use a one or two SDO line configuration.
[b] DP protocol sample frequency limitation: cannot support >48 kHz; i.e., does not support 88.2 kHz, 96 kHz, 176.4 kHz and 196 kHz.

1.7 Security

1.7.1 Security Controller (TSEC)

TSEC heavy-secure (HS) hardware is capable of authenticating its own code autonomously using its Secure Boot ROM and signature verification keys. Integrated secure memory enables tamper resistant secure storage and transaction verification. TSEC implements a random number generator (RNG), and has a Falcon engine that supports AES-128b; no other cryptographic primitives or key sizes are supported. Two independent instruction queues (capable of holding up to 16 instructions) are used to provide encryption support for DRM schemes, including protected content encryption/decryption. Two instances of the TSEC controller (i.e., TSECA and TSECB) balance performance requirements of increasingly demanding use cases.

Features:

- TSECA – performs GSC blob signing for NVDEC
- TSECA/B
    - Communicates with SE for any crypto acceleration, if required.
    - Side channel counter-measures for AES.
    - Dedicated video protection region in memory
- Programmable in the memory controller
- Extends security controller i-cache and d-cache
- Only accessible by the Security Controller
- Minimum size requirements avoid security exposure

1.7.2 Security Engine

A dedicated platform security engine supports secure boot, incorporates a NIST SP800-90 complaint random number generator (RNG) including built in ring oscillator based entropy source used to seed a deterministic random bit generator (DRBG), and a protected memory aperture for video use cases.

Features:

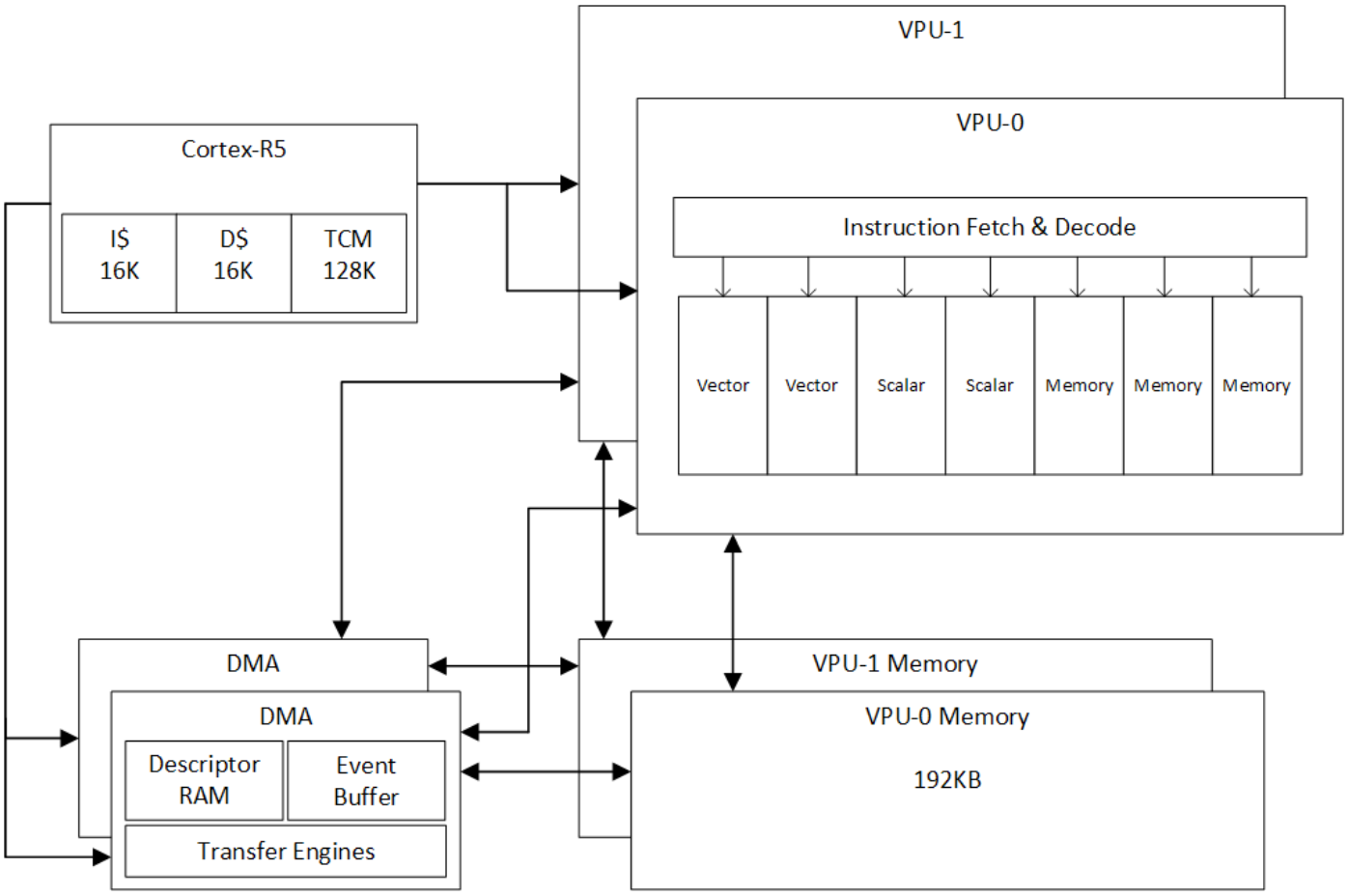
- Side channel attack prevention
- Encryption of memory traffic
- RSA PKC 2048-bit CMAC based boot support
- Support for multiple security domains throughout the control plane and peripheral bridges
- AES-128/192/256 encryption and decryption support
- SHA-1, SHA-224, SHA-256, SHA-384, and SHA-512 support
- RSA: 512, 768, 1024, 1536, 2048, 3072, and 4096-bit support
- ECC: 160, 192, 224, 256, 384, 512, and 521-bit support

1.8 Vision Accelerator

Two Vision Accelerator engines offload computer vision algorithms such as feature detection and matching, optical flow, stereo disparity block matching, and point cloud processing. These application-specific instruction vector processors are a good match for predictable processing, low latency and low power requirements. Imaging filters such as convolutions, morphological operators, histogramming, color space conversion, and warping are ideal applications for these accelerators.

Each Vision Accelerator includes a Cortex-R5 core for command and control, two vector processing units (each with 192KB of on-chip vector memory), and two DMA units for data movement. The 7-way vector processing units contain slots for two vector, two scalar, and three memory operations per instruction.

Figure 1 Vision Accelerator Block Dagram



1.9 Deep Learning Accelerator

The Deep Learning Accelerator (DLA) is a new fixed function engine used to accelerate inference operations on convolution neural networks (CNNs). The DLA supports accelerating some or all desired CNN layers such as convolution, activation, pooling, local response normalization, and full-connected layers.

> Visit the NVDLA Open Source Project (nvdla.org) for additional information on deep learning, convolution neural networks, and accelerating deep learning inference operations.

DLA hardware is comprised of the following components:

1. Convolution Core – optimized high-performance convolution engine.
   Convolution operations work on two sets of data: one set of offline-trained “weights” (which remain constant between each run of inference), and one set of input “feature” data (which varies with the network’s input). The convolutional engine exposes parameters to map many different sizes of convolutions onto the hardware with high efficiency.
2. Single Data Point Processor – single-point lookup engine for activation functions.
   The Single Data Point Processor (SDP) allows for the application of both linear and non-linear functions onto individual data points. This is commonly used immediately after convolution in CNN systems. The SDP has a lookup table to implement non-linear functions, or for linear functions it supports simple bias and scaling. This combination can support most common activation functions, as well as other element-wise operations, including ReLU, PReLU,

precision scaling, batch normalization, bias addition, or other complex non-linear functions, such as a sigmoid or a hyperbolic tangent.

3. Planar Data Processor – planar averaging engine for pooling.
   The Planar Data Processor (PDP) supports specific spatial operations that are common in CNN applications. It is configurable at runtime to support different pool group sizes, and supports three pooling functions: maximum-pooling, minimum-pooling, and average-pooling.
4. Cross-Channel Data Processor – multi-channel averaging engine for advanced normalization functions.
   The Cross-channel Data Processor (CDP) is a specialized unit built to apply the local response normalization (LRN) function – a special normalization function that operates on channel dimensions, as opposed to the spatial dimensions.
5. Data Reshape Engines – memory-to-memory transformation acceleration for tensor reshape and copy operations.
   The data reshape engine performs data format transformations (e.g., splitting or slicing, merging, contraction, reshape-transpose). Data in memory often needs to be reconfigured or reshaped in the process of performing inferencing on a convolutional network. For example, “slice” operations may be used to separate out different features or spatial regions of an image, and “reshape-transpose” operations (common in deconvolutional networks) create output data with larger dimensions than the input dataset.
6. Bridge DMA – accelerated path to move data between two non-connected memory systems.
   The bridge DMA (BDMA) module provides a data copy engine to move data between the system DRAM and the dedicated memory interface.

1.10 Safety Cluster Engine

The Safety Cluster Engine (SCE) is a general-purpose computing subsystem based on an ARM® Cortex® -R5 and it is intended to act as a functional safety management processor. The SCE subsystem provides all of the necessary hardware features to provide fault management capabilities. The cluster consists of two Cortex-R5 processor cores with a tightly-coupled RAM, support peripherals (e.g., timers, interrupt controller), and routing logic. The Cortex-R5 core used in SCE includes floating point and double precision floating point capabilities. In safety applications, the two SCE Cortex-R5 cores operate in lockstep mode and function as a single core with comparison logic to detect any differences between their operations. However, the redundant SCE Cortex-R5 core can be disabled when not required, and this is the default state. The SCE does not support operating each Cortex-R5 independently.

1.11 Interface Descriptions

1.11.1 SD/eMMC Controller

Standard	Notes
SD Specifications, Part A2, SD Host Controller Standard Specification, Version 4.1	
SD Specifications, Part 1, Physical Layer Specification, Version 4.2	
SD Specification, Part 1, eSD (Embedded SD) Addendum, Version 2.10	
SD Specifications, Part E1, SDIO Specification Version, 4.1	Support for SD 4.0 Specification without UHS-II
JEDEC Standard, Embedded Multimedia Card (e•MMC) Electrical Standard 5.1	JESD84-B51

The SecureDigital (SD)/Embedded MultiMediaCard (eMMC) controller is capable of interfacing to an external SD card or SDIO device, and provides the interface for the on-module eMMC. It has a direct memory controller interface and is capable of initiating data transfers between system memory and an external card or device. It also has an APB slave interface to access its configuration registers. To access the on-system RAM for MicroBoot, the SD/MMC controller relies on the path to System RAM in the memory controller.

Features:

- 8-bit data interface to on-module eMMC
- 4-bit data interface for SD cards/SDIO
- Supports card interrupts for SD cards (1/4/8-bit SD modes) and SDIO devices
- Supports read wait control and suspend/resume operation for SD cards
- Supports FIFO overrun and underrun condition by stopping SD clock
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TB.

1.11.2 Universal Flash Storage Complex

Standard	Notes
JEDEC Standard: Universal Flash Storage (UFS), Version 2.0 - JESD220B	
JEDEC Standard: Universal Flash Storage Host Controller Interface (UFSHCI), Version 2.0 - JESD223B	
MIPI Alliance Specification for M-PHY, Version 3.1	
MIPI Alliance Specification for UniPro, Version 1.6	

The Universal Flash Storage (UFS) Complex in JAX series module is comprised of the following blocks:

- A Universal Flash Storage Host Controller (UFSHC)
- A MIPI Unified Protocol (UniPro) interface controller
- Two MIPI M-PHY (MPHY) high-speed serial interfaces

The Universal Flash Storage (UFS) complex can be operated in either single (x1) or dual (x2) lane configurations to support operations at HS-G1, HS-G2, and HS-G3 with both Rate A and Rate B speeds. MPHY modules drive the physical link; they convert the parallel data streams from the high speed serializer into high-speed differential or low-speed PWM-like transmissions.

Features:

- 32 Transfer request slots and eight task management slots
- Max throughput 1168 MBps @ latency 1.2 µs @ LV/SS/25C, for G3x2 RATEB per direction
- LS-MODE PWM-G1~G4 (for x1 and x2 configurations)
- HS-MODE HS-G1~G3 (for x1 and x2 configurations)
- Polarity inversion supported via M-TX configuration attribute programming
- LANE reversal
- Clock gating
- Reference clock frequency to UFS device
- 19.2/26 – 19.2 MHz is default

1.11.3 USB Complex

Standard	Notes
Universal Serial Bus Specification Revision 3.1	Host mode only
Universal Serial Bus Specification Revision 3.0	Device mode only
Universal Serial Bus Specification Revision 2.0	• USB Battery Charging Specification, version 1.2; including Data Contact Detect protocol • Modes: Host and Device • Speeds: Low, Full, High
Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0	

1.11.3.1 USB Controller

The JAX series module integrates both an xHCI controller and USB 3.0 device controller. The xHCI controller supports the xHCI programming model for scheduling transactions and interface managements as a host that natively supports USB 3.1, USB 2.0, and USB 1.1 transactions with its USB 3.1 and USB 2.0 interfaces. The USB 3.0 device controller enables the JAX series module to be accessed from an external host device. The USB 3.0 device controller supports USB 2.0 or USB 3.0 with up to 15 IN and 15 OUT endpoints, where a control endpoint consists of one bidirectional endpoint; endpoints can be configured by the driver to support transfer types of different device classes such as modem, storage, or input devices. Both the xHCI controller and USB 3.0 device controller support USB link power management; and both controllers support remote wakeup, wake on connect, wake on disconnect, and wake on over current in all power states, including deep sleep mode.

1.11.3.2 USB 2.0 Operation

Each USB 2.0 port operates in USB 2.0 High-Speed mode when connecting directly to a USB 2.0 peripheral or in USB 1.1 Full- and Low-Speed modes when connecting directly to a USB 1.1 peripheral. When operating in High-Speed mode, **each** USB 2.0 port is allocated with one High-Speed unit bandwidth; ~480 Mb/s theoretical bandwidth is allocated to each USB 2.0 port. When operating in Full- or Low-Speed modes **all** USB 2.0 ports share one Full/Low-Speed unit bandwidth; ~12 Mb/s theoretical bandwidth is distributed across these ports.

All USB 2.0 ports support software initiated L1 and L2 (suspend) link power management. USB 2.0 ports do not support hardware initiated L1 link power management.

1.11.3.3 USB 3.1 (Host) Operation

USB 3.1 ports support both Generation 1 - SuperSpeed USB and Generation 2 - SuperSpeed USB 10Gbps transfer rates. USB 3.1 port 0 and port 3 share one 10Gbps unit bandwidth, while USB 3.1 is allocated a separate 10Gbps unit bandwidth.

All USB 3.1 ports support hardware initiated U1 and U2 link power management as well as software initiate U3 (suspend) link power management.

1.11.4 PCIe

Standard	Notes
PCI Express® Base Specification Revision 4.0, Version 0.7	
PCI Express® Card Electromechanical Specification Revision 4.0, Version 0.5	

The JAX series module integrates a PCIe 4.0 compliant root port controller based on the Synopsys DesignWare PCIe Dual-Mode Controller; supports Gen1, Gen2, Gen3, and Gen4 link speeds (up to 16Gbps) with a 256-byte maximum payload size. Dual-mode controller supports PCIe endpoint mode operation and incorporates an integrated DMA engine to help to offload CPU workload by performing DMA data transfer.

Features:

- PCIe controller configurations:
  - x8 lane controller (C5)
    - Supports x8, x4, x2, and x1 links
    - Supports lane reversal for x8, x4 or x2 and lane flipping for x4, x2 or x1
    - Supports both root port and endpoint modes
  - x4 lane controller (C0)
    - Supports x4, x2, and x1 links
    - Supports lane reversal for x4 or x2 and lane flipping for x2 or x1
    - Root port operations only
  - x2 lane controller (C4)
    - Supports x2 and x1 links
    - Supports lane reversal for x2 and lane flipping for x1
    - Root port operations only
  - x1 lane controller (C1, C3)
    - Supports x1 links
    - Root port operations only
- PCIe messages and message signaled interrupt (MSI/MSI-X):
  - Reporting received messages in either root port or endpoint mode
  - Generating messages in either root port or endpoint mode
  - Reporting received MSI/MSI-X in root port mode and generating MSI/MSI-X in endpoint mode
- PCIe link low power states:
  - Support L0s, L1, L1 sub-states, and L2/3 link low power states
  - Support link speed management
- PCIe capabilities and services:
  - Hot-plug (via virtual GPIO)
  - Advanced error reporting (AER)
  - Latency tolerance reporting (LTR)

1.11.5 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) controller allows a duplex, synchronous, serial communication between the controller and external peripheral devices; it supports both Master and Slave modes of operation on the SPI bus. Software can program the controller to generate transactions of a required number of packets of specific packet size on the SPI bus, where a transaction is a sequence of packets in either direction.

JAXi: SPI2 is reserved for Safety MCU communication when required. If there are no system safety requirements SPI2 can be made available for other purposes so long as SPI2 CS is held high during reset to prevent IST boot loop.

Two modes of operation:

- PIO Mode - requires software to read and write FIFOs for handling data transfers between system memory and FIFO.
- DMA Mode - uses a channel of the General-Purpose DMA controller (outside of SPI) to transfer data between system memory and the FIFOs.

At the end of each transaction, an Interrupt is generated, if enabled. Software uses Tx and Rx operations in combination with Chip Select (CS) controls to generate commands on the SPI bus.

Features:

- Maximum Data Rate: 65 Mbps in Master Mode, 50 Mbps in Slave Mode
- Master Mode Operation
  - All transfer modes (Mode 0, Mode 1, Mode 2, Mode 3) supported for both Tx and Rx transactions
- Slave Mode Operation
  - Slave Tx: Mode 1 and Mode 3 supported
  - Slave Rx: All transfer modes (Mode 0, Mode 1, Mode 2, Mode 3) supported
- Independent Rx and Tx FIFO
- FIFO Size: 64 x 32 bits
- Programmable packet sizes of 4 to 32 bits
- Packed and Unpacked Mode
  - Four Packed Packet Sizes:
    - Master: 4, 8, 16, 32 bits
    - Slave: 8, 16, 32 bits
  - Unpacked Packet Size
    - Master: 4 ~ 32 bits
    - Slave: 8 ~ 32 bits
- PIO or DMA Mode depending on total transfer sizes and packet size
  - PIO Mode: transfer sizes <= 64 words (32-bit)
  - DMA Mode: transfer sizes > 64 words (32-bit); limited to 64 Kb words (32-bit) per transfer
- Programmable Clock Phase and Polarity
- Programmable Delay between Consecutive Transfers
- Chip select (CS) Controllable by Software or Generated by Hardware on Packet Boundaries
- Maximum 4-chip Support with Programmable CS Polarity for Each Chip Select

Figure 2 SPI Master Timing Diagram

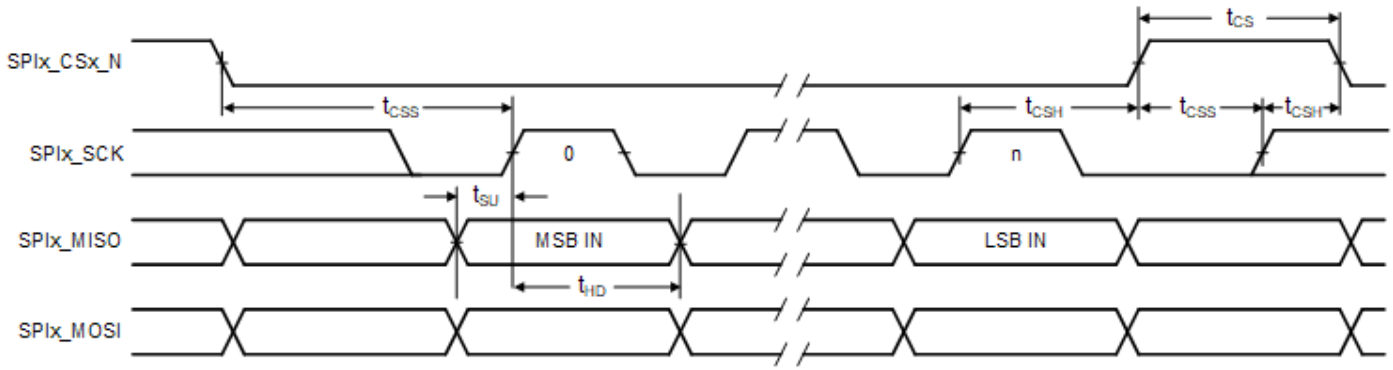


Table 9 SPI Master Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
Fsck	SPIx_SCK clock frequency			65	MHz
Psck	SPIx_SCK period	1/Fsck			ns
t_{CH}	SPIx_SCK high time	50%Psck -10%		50%Psck +10%	ns
t_{CL}	SPIx_SCK low time	50%Psck -10%		50%Psck +10%	ns
t_{CRT}	SPIx_SCK rise time (slew rate)	0.1			V/ns
t_{CFT}	SPIx_SCK fall time (slew rate)	0.1			V/ns
t_{SU}	SPIx_MISO setup to SPIx_SCK rising edge	2			ns
t_{HD}	SPIx_MISO hold from SPIx_SCK rising edge	3			ns
t_{CSS}	SPIx_CSx_N setup time	2			ns
t_{CSH}	SPIx_CSx_N hold time	3			ns
t_{CS}	SPIx_CSx_N high time	10			ns

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

Figure 3 SPI Slave Timing Diagram

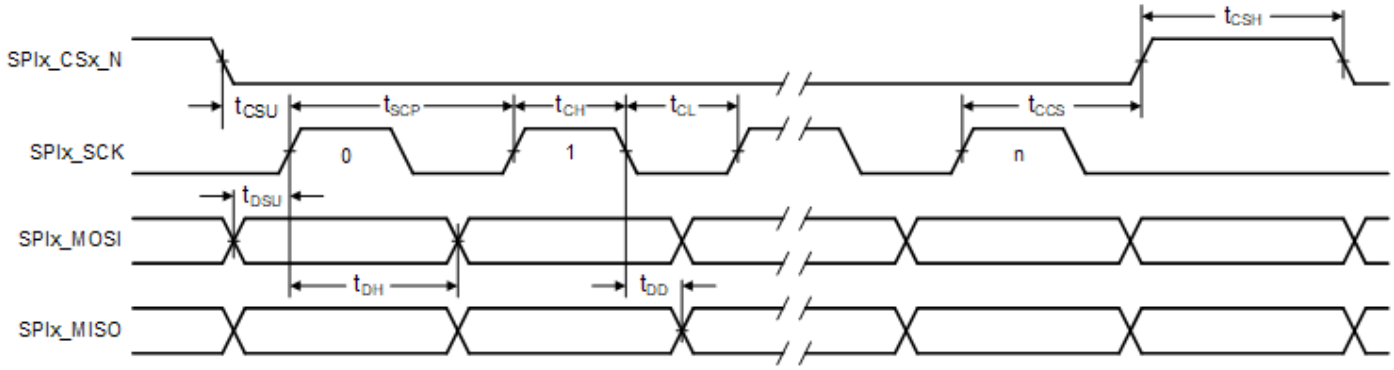


Table 10 SPI Slave Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCP}	SPIx_SCK period	$2*(t_{SDD}+ t_{MSU}$[1]$)$			ns
t_{SCH}	SPIx_SCK high time	$t_{SDD} + t_{MSU}$[1]			ns
t_{SCL}	SPIx_SCK low time	$t_{SDD} + t_{MSU}$[1]			ns
t_{SCSU}	SPIx_CSx_n setup time	1			t_{SCP}
t_{SCSH}	SPIx_CSx_n high time	1			t_{SCP}
t_{SCCS}	SPIx_SCK rising edge to SPIx_CSx_n rising edge	1		1	t_{SCP}
t_{SDSU}	SPIx_MOSI setup to SPIx_SCK rising edge	1		1	ns
t_{SDH}	SPIx_MOSI hold from SPIx_SCK rising edge	2		11	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge	3.5		16	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge	3		13	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge	4		17	ns

1. t_{MSU} is the setup time required by the external master

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

1.11.6 Quad Serial Peripheral Interface Controller - (JAXi only)

Not supported on JAX modules

The Quad Serial Peripheral Interface (QSPI) controller interfaces with the on-board (NOR) flash memory used as the boot device for JAXi modules. This controller provides a multi-bit serial communications link between the application processor and the flash memory. The QSPI interface is a serial protocol extension of the industry standard Serial Peripheral Interface (SPI) protocol over 1, 2, or 4 data lanes.

QSPI controller is variation of SPI controller with the following exceptions:

- Master mode only, no support for slave mode.
- Half-duplex communication only, no support for full-duplex communication.

QSPI controller interface timing specification is the same as SPI interface timing (Max Speed: 65 MHz).

Features:

- Supports secure SPI NOR
- Single (x1) Mode, Dual (x2) Mode, Quad (x4) SDR and DDR Flash Mode
- Independent Rx and Tx FIFO
- FIFO Size: 64 x 32 bits
- PIO or DMA Mode depending on total transfer sizes
    - PIO Mode: transfer sizes <= 64 words (32-bit)
    - DMA Mode: transfer sizes > 64 words (32-bit); limited to 256 Mi words (32-bit) per transfer
- Byte-aligned and Packet-based (Packet Size = 8, 16, 32 bits) Packed and Unpacked Mode
    - Packed Mode only for 8-bit and 16-bit packets
    - Packed Mode's minimum transfer size: 32 bits (one FIFO word)
    - 32-bit packets always packed by definition; sending such packets in Packed and Unpacked Mode thus effectively the same
    - Unpacked Mode always used for transfer sizes less than 32 bits
- 1.8V QSPI flash devices

1.11.7 Universal Asynchronous Receiver/Transmitter (UART)

UART controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be checked by the receiver for any transmission bit errors.

Features:

- Synchronization for the serial data stream with start and stop bits to transmit data and form a data character
- Supports both 16450- and 16550-compatible modes. Default mode is 16450
- Device clock up to 200MHz, baud rate of 12.5Mbits/second
- Data integrity by attaching parity bit to the data character
- Support for word lengths from five to eight bits, an optional parity bit and one or two stop bits
- Support for modem control inputs
- DMA capability for both TX and RX
- 8-bit x 36 deep TX FIFO
- 11-bit x 36 deep RX FIFO. 3 bits of 11 bits per entry will log the RX errors in FIFO mode (break, framing and parity errors as bits 10,9,8 of FIFO entry)

- Auto sense baud detection
- Timeout interrupts to indicate if the incoming stream stopped
- Priority interrupts mechanism
- Flow control support on RTS and CTS
- Internal loopback
- SIR encoding/decoding (3/16 or 4/16 baud pulse widths to transmit bit zero)

1.11.8 Controller Area Network (CAN)

Standard	Notes
ISO/DIS 16845-2	CAN conformance test
ISO 11898-1:2015	Data link layer and physical signalling; CAN FD Frame formats
ISO 11898-4:2004	Time-triggered communication

The JAX series module integrates the Bosch Time-triggered Controller Area Network (M_TTCAN) controller version 3.2.0. Two independent CAN ports/channels supports connectivity to two CAN networks; each port instantiates the Bosch M_TTCAN module, a message RAM module, an APB slave interface module, interrupt aggregator, time-triggered control module and a wake detect module. All M_TTCAN external modules have direct connections to M_TTCAN except for the wake detect module.

Features:

- Standard frame and extended frame transmission/reception enable.
- Transfer rate: programmable bit rate up to 15Mbps.
- 0 – 8 byte data length, with the ability to receive the first 8 bytes when Data length coding is > 8 Bytes
- 32 message buffers per channel
- Prioritization of transmit buffers.
- Receive/transmit history list function
- Automatic block transmission function
- Multi-buffer receive block function
- Flexible maskable identifier filter supports of two 32-bit, or four 16-bit, or eight 8-bit filters for each channel
- Programmable data bit time, communication baud rate and sample point.
    - As an example the following sample-point configurations can be configured: 66.7%, 70.0%, 75.0%, 80.0%, 81.3%, 85.0%, 87.5%
    - Baud rates in the range of 10kbps up to 1000kbps can be configured
- Enhanced features:
    - Each message buffer can be configured to operate as a transmit or a receive message buffer
    - Transmission priority is controlled by the identifier or by mailbox number (selectable)
    - A transmission request can be aborted by clearing the dedicated Transmit-Request flag of the concerned message buffer.
    - Automatic block transmission operation mode (ABT)
    - Time stamp function for CAN channels 0 to n in collaboration with timers
- Release from bus-off state by software.
- Wake-Up with integrated low pass filter (debounce) option to prevent short glitches on CAN bus, through CAN RX signal toggling from CAN transceiver
    - For normal operation (after wake) there is a digital filter in the CAN controller
- Listen-Only mode to monitor CAN bus
- Wake-up signal to both internal and external (either interrupt signal or GPIO) to initiate power up if needed.
    - Ready to receive the first CAN message within 10ms of wake event generated by the CAN master.

    - Ready to transmit the first CAN message within 50ms of wake event generated by the CAN master.
- Loop Back for self-test.

1.11.9 Reduced Gigabit Media Independent Interface (RGMII)

Standard	Notes
Reduced Gigabit Media Independent Interface (RGMII) Specification, Version 2.6	Timing complies with the original RGMII mode in version 2.0 of specification
IEEE 1588-2008	Precision networked clock synchronization
IEEE 802.3az-2010	Energy Efficient Ethernet (EEE)
IEEE 802.1as-2011	Timing and synchronization for time-sensitive applications in bridged LANs
IEEE 802.1Qat/Qav	Virtual Bridged LANs
IEEE 1722-2011	Layer 2 transport protocol for time sensitive apps in bridged LANs
IEEE 802.1Q	VLAN tag filtering of RX packets

JAX series modules integrate an Ethernet controller/MAC with AVB support, and provides a Reduced Gigabit Media Independent Interface (RGMII). The transmit clock signal is provided by the MAC and is synchronous with the data signals.

Controller Features:

- Ethernet speeds of 10/100/1000 Mbps
- One channel (channel 0) for legacy, best-effort Ethernet traffic on transmit interface.
- Support for a maximum of four queues at 100 Mbps and 1000 Mbps.
- Support for frames of up to 9 KB
- Support for serial Management Interface MDIO, MDC.
- Forwarding RX multicast/broadcast packets to multiple queues.
- Audio synchronized to network time.
- Low predictable latency for audio packet processing.

TX and RX Features:

- Separate transmission, reception, and control interfaces to the application
- Configurable big-endian and little-endian mode for Transmit and Receive paths
- Half-duplex operation:
    - CSMA/CD Protocol support
    - Flow control (using back-pressure support)
    - Packet bursting and packet extension in 1000 Mbps half-duplex operation
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- Optional network statistics with RMON or MIB Counters (RFC2819/RFC2665)
- Ethernet packet time-stamping (64-bit timestamps given in the TX or RX status of PTP packet). Both one-step and two-step time-stamping is supported in TX direction.

2 Power and System Management

The Power Management Controller (PMC) primarily manages voltage transitions for the module as it transitions to/from different low power modes. It provides power-gating controls for the SOC partitions, integrates dedicated hardware (Wake Engine) to consolodate wake management related functions, includes scratch storage to preserve context during sleep modes when CPU and/or SOC power rails are off, and interacts with external PMIC device through sideband signals. Additional CPU power gating and rail gating controls along with Flow Controller logic are contained within the CPU complex (CCPLEX). Module power (i.e., VIN) is comprised of two inputs: SYS_VIN_HV (9V – 20V), SYS_VIN_MV (5V). VIN must be supplied by the carrier board that the module is designed to connect to. All interfaces are referenced to on-module voltage rails, additional IO voltage is not required to be supplied to the module. See the *Jetson* AGX *Xavier Series Module Product Design Guide* for details on connecting to each of the interfaces.

2.1 VCC_RTC

An optional back up battery can be attached to the VCC_RTC module input to maintain the module real-time clock (RTC) when VIN is not present. This pin is connected directly to the onboard PMIC. Details of the types of backup cells that optionally can be connected are found in the PMIC manufacturer's data sheet. When a backup cell is connected to the PMIC, the RTC will retain its contents and can be configured to charge the backup cell as well.

The following backup cells may be attached to this pin:

- Super Capacitor (gold cap, double layer electrolytic)
- Standard capacitors (tantalum)
- Rechargeable Lithium Manganese cells

The backup cells must provide a voltage in the range 2.5V to 3.5V (constant current of 2.0µA for 2.5V; 2.3µA for 3.3V typical; 10µA maximum). These will be charged with a constant current, and a constant voltage charger that can be configured between 2.5V and 3.5V (constant voltage) output and 50 uA to 800 uA (constant current).

A voltage range of 2.5V to 3.5V is supported on both JAX and JAXi modules, but may not be compatible with future modules. To be compatible with future modules of the same connector, 3.3V should be used.

2.2 Power Sequencing

JAX series modules and the product carrier board **MUST** be power sequenced properly to avoid potential damage to components on either the module or the carrier board system.

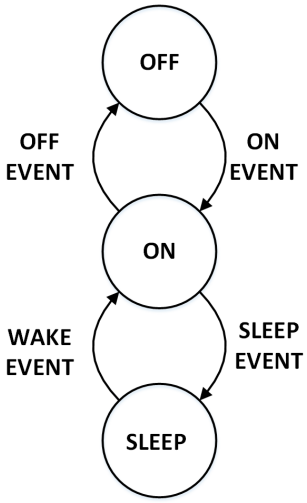
The JAX series module **MUST** be powered before the main carrier board circuits. The CARRIER_POWER_ON signal is generated by the module and passed to the carrier board to indicate that the module is powered up and that the power up sequence for the carrier board circuits can begin. During power up, the carrier board **MUST** wait until the signal CARRIER_POWER_ON is asserted from the module before enabling its power. The module will de-assert the SYS_RESET_N signal to enable the complete system to boot. On receiving a Shutdown request the module will assert the SYS_RESET_N signal, allowing the carrier board to put any components into a known state. The CARRIER_POWER_ON signal will then be de-asserted to indicate to the carrier board to power down. The carrier board **MUST** disable its power at this point; the module will then disable its power and shut down. In order to meet the Power Down requirements, discharge circuitry is required.

Refer to the J*etson AGX Xavier Series Module Product Design Guide* for system level details on the application of power, power sequencing and monitoring.

2.3 Power States

The JAX series module operates in three main power modes: OFF, ON, and SLEEP. Transitions between these states are based on various events from hardware or software.

Figure 4 Power State Transition Diagram



2.3.1 ON State

The ON power state is entered from either OFF or SLEEP states. In this state, JAX series modules are fully functional and will operate normally. An ON event has to occur for a transition between OFF and ON states. The only ON EVENT currently used is a low to high transition on the POWER_BTN_N pin. This must occur with VDD_IN connected to a power rail, and VDDIN_PWR_BAD_N is asserted (at a logic1). The VDDIN_PWR_BAD_N control is the carrier board indication to the JAX module that the VIN power is good. The carrier board should assert this high only when VIN has reached its required voltage level and is stable. This prevents JAX series modules from powering up until the VIN power is stable.

2.3.2 OFF State

The OFF state is the default state when the system is not powered. It can only be entered from the ON state or through an OFF event.

OFF Events

Event	Details	Preconditions
Power Button	Keeping POWER_BTN# low for 10 seconds will power down the module	In ON State
SW Shutdown	Software will initiate	ON state, software operational
Thermal Shutdown	If the internal temperature of the module reaches an unsafe temperature, the hardware is designed to initiate a shutdown	Any power state

Event	Details	Preconditions
Voltage Brown out	A voltage monitor circuit is implemented on the module to indicate if the main DC input rails (VIN_SYS_HV, VIN_SYS_MV) “droop” below an acceptable level; if this occurs, the hardware is designed to initiate a shutdown. Power detection is signaled from the carrier board through the VIN_PWR bad, the VIN_SYS_HV (5V to 20V) and VIN_SYS_MV (5V +/- 10%).	Any power state

2.3.3 SLEEP State

The SLEEP state can only be entered from the ON state. This state allows the module to quickly resume to an operational state without performing a full boot sequence. The SLEEP state also includes a low power mode SC7 (deep sleep) where the module operates only with enough circuitry powered to allow the device to resume and re-enter the ON state. During this state the output signals from the module are maintained at their logic level prior to entering the state (i.e., they do not change to a 0V level). To exit the SLEEP state a WAKE event must occur; WAKE events can occur from within the module or from external devices through various pins on the module connector.

SLEEP and WAKE Events

Event	Details
RTC WAKE up	Timers within the module can be programmed, on SLEEP entry. When these expire they will create a WAKE event to exit the SLEEP state.
Thermal Condition	If the module internal temperature exceeds programmed hot and cold limits the system will be force to wake up, so it can report and take appropriate action (shut down for example)
Low Power	If a power input voltage drops below a set voltage (e.g., 6V) then the system can be woken up to initiate a graceful shutdown.
USB VBUS detection	If VBUS is applied to the system (USB cable attached) then the device can be configured to Wake and enumerate
SD Card detect	The Card detect pin may be configured to enable the system to wake.
Module connector Interface WAKE signal	Programmable signals on the module connector.

Programmable WAKE Pins

Potential Wake Event (Reference Design Signal)	Module Pin Assignment	Wake #
PCIe L2 Clock Request (PEX_L2_CLKREQ_N)	PEX_C2_CLKREQ_N	Wake00
PCIe Wake Request (PEX_WAKE_N)	PEX_WAKE_N	Wake01
SD Card Data 1 (SDCARD_D1)	SDCARD_D1	Wake03
Backlight PWM (BKLIGHT_PWM)	GPIO27	Wake04

Potential Wake Event (Reference Design Signal)	Module Pin Assignment	Wake #
GPIO 0 (CVB_GPIO0)	GPIO02	Wake08
System Overcurrent Control (SYSTEM_OC#)	SYSTEM_OC_N	Wake10
GPIO 1 (CVB_GPIO1)	GPIO11	Wake12
GPIO 3 (GPIO3/SD_WP)	GPIO29	Wake13
NVIDIA Debug Select (NVDBG_SEL)	NVDBG_SEL	Wake14
GPIO 2 (CVB_GPIO2)	GPIO12	Wake15
Ethernet SMA MDIO (RGMII_SMA_MDIO)	RGMII_SMA_MDIO	Wake17
Ethernet Interrupt (ENET_INT)	ENET_INT	Wake20
I2C General Purpose 3 Data (I2C_GP3_DAT)	I2C3_DAT	Wake21
I2C General Purpose 4 Data (I2C_GP4_DAT)	I2C4_DAT	Wake22
Safe State (SAFE_STATE)[1]	GPIO31	Wake25
Voltage Monitor (VMON)	VCOMP_ALERT_N	Wake26
Ethernet RX Control (RGMII_RX_CTL)	RGMII_RX_CTL	Wake28
Power On (POWER_ON)	POWER_BTN_N	Wake29
GPU Fault (GPU_FAULT)	GPIO01	Wake30
I2C General Purpose 1 Data (I2C_GP1_DAT)	I2C1_DAT	Wake31
PCIe L5 Clock Request (PEX_L5_CLKREQ_N)	PEX_C5_CLKREQ_N	Wake32
Board Identification 1 (BOARD_ID1)	UART1_CTS	Wake33
GPIO Expander 0 Interrupt (GPIO_EXP0_INT)	GPIO32	Wake34
USB OTG Identification (USB_OTG_ID)	GPIO30	Wake35
GPIO Expander 1 Interrupt (GPIO_EXP1_INT)	GPIO33	Wake36

Potential Wake Event (Reference Design Signal)	Module Pin Assignment	Wake #
GPIO Expander 2 Interrupt (GPIO_EXP2_INT)	GPIO34	Wake37
Watchdog Timer Reset Output (WDT_RESET_OUT)	WDT_RESET_OUT_N	Wake38
SPI 2 Chip Select 0 (SPI2_CS0#)	SPI2_CS0_N	Wake39
GPIO 5 (CVB_GPIO5)	GPIO17	Wake40
I2C General Purpose 2 Data (I2C_GP4_DAT)	I2C2_DAT	Wake41
CAN 1 Data Input (CAN1_DIN)	CAN1_DIN	Wake42
CAN 0 Data Input (CAN0_DIN)	CAN0_DIN	Wake43
SPI 3 Clock (SPI3_CLK)	SPI3_CLK	Wake44
SPI 1 Chip Select 0 (SPI1_CS0#)	SPI1_CS0_N	Wake45
CAN 0 GPIO 1 (CAN0_GPIO1)	GPIO07	Wake46
CAN1 GPIO 1 (CAN1_GPIO1)	GPIO10	Wake48
SPI 1 Chip Select 1 (SPI1_CS1#)	SPI1_CS1_N	Wake50
Fan Tachometer (FAN_TACH)	FAN_TACH	Wake51
UART 1 Clear to Send (UART1_CTS)	UART2_CTS	Wake52
UART 2 Clear to Send (UART2_CTS)	UART5_CTS	Wake53
PCIe L1 Clock Request (PEX_L1_CLKREQ_N)	PEX_C1_CLKREQ_N	Wake54
PCIe L4 Clock Request (PEX_L4_CLKREQ_N)	PEX_C4_CLKREQ_N	Wake55
SPI 3 Chip Select 0 (SPI3_CS0#)	SPI3_CS0_N	Wake56
SATA Device Sleep (SATA_DEV_SLP)	SATA_DEV_SLP	Wake57
SPI 3 Chip Select 1 (SPI3_CS1#)	SPI3_CS1_N	Wake58
Discrete GPU Alert (DGPU_ALERT)	GPIO03	Wake59

Potential Wake Event (Reference Design Signal)	Module Pin Assignment	Wake #
DP 0 Hot-Plug-Detect (DP0_HPD)	DP0_HPD	Wake60
(USB_VBUS_EN0)	GPIO22	Wake61
(USB_VBUS_EN1)	GPIO23	Wake62
DP 1 Hot-Plug-Detect (DP1_HPD)	DP1_HPD	Wake63
Discrete GPU Over-Temperature (DGPU_OVERT)	OVERTEMP_N	Wake64
PCIe L3 Clock Request (PEX_L3_CLKREQ_N)	PEX_C3_CLKREQ_N	Wake65
GPIO 6 (CVB_GPIO6)	GPIO24	Wake66
Force Recoverry (FORCE_RECOVERY)	FORCE_RECOVERY_N	Wake67
Sleep (SLEEP#)	STANDBY_REQ_N	Wake68
Battery Low (BATLOW#)	GPIO28	Wake69
HDMI Consumer Electronics Control (HDMI_CEC)	HDMI_CEC	Wake70
DP 2 Hot-Plug-Detect (DP2_HPD)	DP2_HPD	Wake71

1. SAFE_STATE - Commonly referred to as 'nSAFE'. Used to indicate that the module has detected an internal error which requires external handling and that correct module operation cannot be trusted at this time. Note, this pin has no relation to the ISO 26262 definition of Safe State.

3 Pin Definitions

The function(s) for each pin on the module is fixed to a single Special-Function I/O (SFIO) or software-controlled General Purpose I/O (GPIO). The JAX series module has multiple dedicated GPIOs; each GPIO is individually configurable as Output/Input/Interrupt sources with level/edge controls. SFIO and GPIO functionality is configured using Multi-purpose I/O (MPIO) pads; each MPIO pad consists of:

- An output driver with tristate capability, drive strength controls and push-pull mode, open-drain mode, or both
- An input receiver with either schmitt mode, CMOS mode, or both
- A weak pull-up and a weak pull-down

MPIO pads are partitioned into multiple “pad control groups” with controls being configured for the group. During normal operation, these per-pad controls are driven by the pinmux controller registers. During deep sleep, the PMC bypasses and then resets the pinmux controller registers. Software reprograms these registers as necessary after returning from deep sleep.

Refer to the *Jetson Xavier OEM Product Design Guide* for more information on pad behavior associated with different interfaces and the *Xavier Series SoC Technical Reference Manual* for more information on modifying MPIO pad controls.

3.1 Power-on Reset Behavior

Each MPIO pad has a deterministic power-on reset (PoR) state. The particular reset state for each pad is chosen to minimize the need of additional on-board components; for example, on-chip weak pull-ups are enabled during PoR for pads which are usually used to drive active-low chip selects eliminating the need for additional pull-up resistors.

The following list is a simplified description of the JAX series module boot process focusing on those aspects which relate to the MPIO pins:

1. System-level hardware executes the power-up sequence. This sequence ends when system-level hardware releases SYS_RESET_N.
2. The boot ROM begins executing and programs the on-chip I/O controllers to access the secondary boot device.
3. The boot ROM fetches the Boot Configuration Table (BCT) and boot loader from the secondary boot device.
4. If the BCT and boot loader are fetched successfully, the boot ROM transfers control to the boot loader.
5. Otherwise, the boot ROM enters USB recovery mode.

3.2 Deep Sleep Behavior

Deep Sleep is an ultra-low-power standby state in which the module maintains much of its I/O state while most of the chip is powered off. During deep sleep most of the pads are put in a state called Deep Power Down (DPD). The sequence for entering DPD is same across pads.

ALL MPIO pads **do NOT** have identical behavior during deep sleep. They differ with regard to:

- Input buffer behavior during deep sleep
  - Forcibly disabled OR
  - Enabled for use as a “GPIO wake event” OR
  - Enabled for some other purpose (e.g., a “clock request” pin)
- Output buffer behavior during deep sleep
  - Maintain a static programmable (0, 1, or tristate) constant value OR
  - Capable of changing state (i.e., dynamic while the chip is still in deep sleep)
- Weak pull-up/pull-down behavior during deep sleep
  - Forcibly disabled OR
  - Can be configured
- Pads that do not enter deep sleep

- Some of the pads whose outputs are dynamic during deep sleep are of special type and they do not enter deep sleep (e.g., pads that are associated with PMC logic do not enter deep sleep, pads that are associated with JTAG do not enter into deep sleep any time.

3.3 Pin List

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
A3	PRSNT0						
A4	SDCARD_D2	SD Card (or SDIO) Data 2			VDDIO_SDMMC1_HV	3.3	Bi-Dir
A5	SDCARD_CMD	SD Card (or SDIO) Command			VDDIO_SDMMC1_HV	3.3	Bi-Dir
A6	UFS0_REF_CLK	UFS Reference Clock			VDDIO_UFS	1.8	Output
A7	GPIO29	GPIO	Wake13		VDDIO_AUDIO	1.8	Bi-Dir
A8	PEX_WAKE_N	PCIe Wake	Wake1		VDDIO_PEX_CTL	1.8	Input
A9	GND	GND					
A10	USB2_P	USB 2.0, Port 2 Data+			AVDD_USB	3.3	Bi-Dir
A11	USB2_N	USB 2.0, Port 2 Data–			AVDD_USB	3.3	Bi-Dir
A12	GND	GND					
A13	GND	GND					
A14	UPHY_RX8_N	UPHY Receive 8-					Input
A15	UPHY_RX8_P	UPHY Receive 8+					Input
A16	GND	GND					
A17	GND	GND					
A18	UPHY_RX4_P	UPHY Receive 4+					Input
A19	UPHY_RX4_N	UPHY Receive 4-					Input
A20	GND	GND					
A21	GND	GND					
A22	UPHY_RX0_P	UPHY Receive 0+					Input
A23	UPHY_RX0_N	UPHY Receive 0-					Input

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
A24	GND	GND					
A25	GND	GND					
A26	NVHS0_SLVS_RX3_P	PCIe/SLVS 0 Receive 3+			DVDDIO_NVHS0	1	Input
A27	NVHS0_SLVS_RX3_N	PCIe/SLVS 0 Receive 3-			DVDDIO_NVHS0	1	Input
A28	GND	GND					
A29	GND	GND					
A30	NVHS0_SLVS_RX7_P	PCIe/SLVS 0 Receive 7+			DVDDIO_NVHS0	1	Input
A31	NVHS0_SLVS_RX7_N	PCIe/SLVS 0 Receive 7-			DVDDIO_NVHS0	1	Input
A32	GND	GND					
A33	GND	GND					
A34	RSVD	-					
A35	RSVD	-					
A36	GND	GND					
A37	GND	GND					
A38	RSVD	-					
A39	RSVD	-					
A40	GND	GND					
A41	CSI2_D0_P	Camera, CSI 2 Data 0+			AVDD_CSI	1.2	Input
A42	CSI2_D0_N	Camera, CSI 2 Data 0–			AVDD_CSI	1.2	Input
A43	GND	GND					
A44	CSI7_D0_P	Camera, CSI_7 Data 0+			AVDD_CSI	1.2	Input
A45	CSI7_D0_N	Camera, CSI_7 Data 0–			AVDD_CSI	1.2	Input
A46	GND	GND					
A47	HDMI_DP1_TX0_P	DisplayPort 1 Lane 0+ or HDMI Lane 2+			AVDDIO_HDMI_DP1	1	Output
A48	HDMI_DP1_TX0_N	DisplayPort 1 Lane 0– or HDMI Lane 2–			AVDDIO_HDMI_DP1	1	Output
A49	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
A50	HDMI_DP2_TX2_N	DisplayPort 2 Lane 2– or HDMI Lane 0–			AVDDIO_HDMI_DP2	1	Output
A51	HDMI_DP2_TX2_P	DisplayPort 2 Lane 2+ or HDMI Lane 0+			AVDDIO_HDMI_DP2	1	Output
A52	GND	GND					
A53	I2C5_CLK	General I2C 5 Clock			VDDIO_EDP	1.8	Bi-Dir
A54	GPIO17	GPIO(GMSI Interrupt 0)	Wake40		VDDIO_CAM	1.8	Bi-Dir
A55	GPIO34	GPIO	Wake37		VDDIO_CAM	1.8	Bi-Dir
A56	SPI1_MISO	SPI 1 Initiator In / Target Out			VDDIO_UART	1.8	Bi-Dir
A57	UART2_CTS	UART 2 Clear to Send	Wake52		VDDIO_UART	1.8	Bi-Dir
A58	GPIO20	GPIO / Boot Strap 2			VDDIO_AUDIO_HV	3.3	Bi-Dir
A59	GPIO05	GPIO / Boot Strap 0			VDDIO_AUDIO_HV	3.3	Bi-Dir
A60	JTAG_TCK	JTAG Test Clock			VDDIO_DEBUG	1.8	Input
A61	SYSTEM_OC_N	Battery Over-current (& Thermal) warning	Wake10		VDDIO_SYS	1.8	Input
A62	GPIO10	GPIO	Wake48		VDDIO_AO_HV	3.3	Bi-Dir
A63	GND	GND					
B3	SYS_VIN_HV_21	System Voltage Input - High				9V-20V	Input
B4	GND	GND					
B5	RGMII_TXC	Ethernet Transmit Clock			VDDIO_EQOS	1.8	Output
B6	SDCARD_CLK	SD Card (or SDIO) Clock			VDDIO_SDMMC1_HV	3.3	Bi-Dir
B7	GND	GND					
B8	GPIO11	GPIO	Wake12		VDDIO_AUDIO	1.8	Bi-Dir
B9	PEX_L1_RST_N	PCIe 1 Reset			VDDIO_PEX_CTL	1.8	Output
B10	RSVD	-					
B11	GND	GND					
B12	UPHY_RX10_P	UPHY Receive 10+					Input

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
B13	UPHY_RX10_N	UPHY Receive 10-					Input
B14	GND	GND					
B15	GND	GND					
B16	UPHY_RX6_P	UPHY Receive 6+					Input
B17	UPHY_RX6_N	UPHY Receive 6-					Input
B18	GND	GND					
B19	GND	GND					
B20	UPHY_RX2_N	UPHY Receive 2-					Input
B21	UPHY_RX2_P	UPHY Receive 2+					Input
B22	GND	GND					
B23	GND	GND					
B24	NVHS0_SLVS_RX1_N	PCIe/SLVS 0 Receive 1-			DVDDIO_NVHS0	1	Input
B25	NVHS0_SLVS_RX1_P	PCIe/SLVS 0 Receive 1+			DVDDIO_NVHS0	1	Input
B26	GND	GND					
B27	GND	GND					
B28	NVHS0_SLVS_RX5_N	PCIe/SLVS 0 Receive 5-			DVDDIO_NVHS0	1	Input
B29	NVHS0_SLVS_RX5_P	PCIe/SLVS 0 Receive 5+			DVDDIO_NVHS0	1	Input
B30	GND	GND					
B31	GND	GND					
B32	RSVD	-					
B33	RSVD	-					
B34	GND	GND					
B35	GND	GND					
B36	RSVD	-					
B37	RSVD	-					
B38	GND	GND					
B39	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
B40	MID4	Module ID 4					
B41	GND	GND					
B42	CSI2_CLK_N	Camera, CSI 2 Clock–			AVDD_CSI	1.2	Input
B43	CSI2_CLK_P	Camera, CSI 2 Clock+			AVDD_CSI	1.2	Input
B44	GND	GND					
B45	CSI7_CLK_P	Camera, CSI_7 Clock+			AVDD_CSI	1.2	Input
B46	CSI7_CLK_N	Camera, CSI_7 Clock–			AVDD_CSI	1.2	Input
B47	GND	GND					
B48	HDMI_DP1_TX1_N	DisplayPort 1 Lane 1– or HDMI Lane 1–			AVDDIO_HDMI_DP1	1	Output
B49	HDMI_DP1_TX1_P	DisplayPort 1 Lane 1+ or HDMI Lane 1+			AVDDIO_HDMI_DP1	1	Output
B50	GND	GND					
B51	HDMI_DP2_TX1_P	DisplayPort 2 Lane 1+ or HDMI Lane 1+			AVDDIO_HDMI_DP2	1	Output
B52	HDMI_DP2_TX1_N	DisplayPort 2 Lane 1– or HDMI Lane 1–			AVDDIO_HDMI_DP2	1	Output
B53	GND	GND					
B54	WDT_RESET_OUT_N	Watchdog Timeout	Wake38		VDDIO_CAM	1.8	Output
B55	GPIO30	GPIO	Wake35		VDDIO_CAM	1.8	Bi-Dir
B56	SPI1_CS1_N	SPI 1 Chip Select 1	Wake50		VDDIO_UART	1.8	Bi-Dir
B57	GND	GND					
B58	GPIO21	GPIO			VDDIO_AUDIO_HV	3.3	Bi-Dir
B59	GPIO04	GPIO / Boot Strap 1			VDDIO_AUDIO_HV	3.3	Bi-Dir
B60	JTAG_TDI	JTAG Test Data In			VDDIO_DEBUG	1.8	Input
B61	CAN1_DIN	CAN 1 Receive		de-glitch		3.3	
B62	GPIO08	GPIO / Digital Mic Input Data			VDDIO_AO_HV	3.3	Bi-Dir
B63	SYS_VIN_HV_15	System Voltage Input				9V-20V	Input

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
C1	SYS_VIN_HV_33					9V-20V	Input
C2	SYS_VIN_HV_26					9V-20V	Input
C3	GND	GND					
C4	RGMII_RD0	Ethernet Receive data bit 0			VDDIO_EQOS	1.8	Input
C5	RGMII_RXC	Ethernet Receive Clock			VDDIO_EQOS	1.8	Input
C6	UFS0_RST_N	UFS Reset			VDDIO_UFS	1.8	Output
C7	I2S1_SDOUT	I2S Audio Port 1 Data Out			VDDIO_AUDIO	1.8	Bi-Dir
C8	PEX_L5_CLKREQ_N	PCIE 5 Clock Request. Input when JAX is Root Port. Output when JAX is Endpoint.	Wake32		VDDIO_PEX_CTL_2	1.8	Bi-Dir
C9	GND	GND					
C10	USB1_N	USB 2.0, Port 1 Data–			AVDD_USB	3.3	Bi-Dir
C11	USB1_P	USB 2.0, Port 1 Data+			AVDD_USB	3.3	Bi-Dir
C12	GND	GND					
C13	GND	GND					
C14	UPHY_RX9_N	UPHY Receive 9-					Input
C15	UPHY_RX9_P	UPHY Receive 9+					Input
C16	GND	GND					
C17	GND	GND					
C18	UPHY_RX5_N	UPHY Receive 5-					Input
C19	UPHY_RX5_P	UPHY Receive 5+					Input
C20	GND	GND					
C21	GND	GND					
C22	UPHY_RX1_N	UPHY Receive 1-					Input
C23	UPHY_RX1_P	UPHY Receive 1+					Input
C24	GND	GND					
C25	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
C26	NVHS0_SLVS_RX2_N	PCIe/SLVS 0 Receive 2-			DVDDIO_NVHS0	1	Input
C27	NVHS0_SLVS_RX2_P	PCIe/SLVS 0 Receive 2+			DVDDIO_NVHS0	1	Input
C28	GND	GND					
C29	GND	GND					
C30	NVHS0_SLVS_RX6_N	PCIe/SLVS 0 Receive 6-			DVDDIO_NVHS0	1	Input
C31	NVHS0_SLVS_RX6_P	PCIe/SLVS 0 Receive 6+			DVDDIO_NVHS0	1	Input
C32	GND	GND					
C33	GND	GND					
C34	RSVD	-					
C35	RSVD	-					
C36	GND	GND					
C37	GND	GND					
C38	RSVD	-					
C39	RSVD	-					
C40	GND	GND					
C41	CSI2_D1_N	Camera, CSI 2 Data 1–			AVDD_CSI	1.2	Input
C42	CSI2_D1_P	Camera, CSI 2 Data 1+			AVDD_CSI	1.2	Input
C43	GND	GND					
C44	CSI5_CLK_P	Camera, CSI 5 Clock+			AVDD_CSI	1.2	Input
C45	CSI5_CLK_N	Camera, CSI 5 Clock–			AVDD_CSI	1.2	Input
C46	GND	GND					
C47	CSI7_D1_P	Camera, CSI_7 Data 1+			AVDD_CSI	1.2	Input
C48	CSI7_D1_N	Camera, CSI_7 Data 1–			AVDD_CSI	1.2	Input
C49	GND	GND					
C50	HDMI_DP2_TX3_N	DisplayPort 2 Lane 3– or HDMI Clk Lane–			AVDDIO_HDMI_DP2	1	Output
C51	HDMI_DP2_TX3_P	DisplayPort 2 Lane 3+ or HDMI Clk Lane+			AVDDIO_HDMI_DP2	1	Output

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
C52	GND	GND					
C53	I2C5_DAT	General I2C 5 Data			VDDIO_EDP	1.8	Bi-Dir
C54	GPIO33	GPIO	Wake36		VDDIO_CAM	1.8	Bi-Dir
C55	GPIO18	GPIO			VDDIO_CAM	1.8	Bi-Dir
C56	UART2_RX	UART 2 Receive			VDDIO_UART	1.8	Bi-Dir
C57	SPI3_CS0_N	SPI 3 Chip Select 0	Wake56		VDDIO_UART	1.8	Bi-Dir
C58	UART2_TX	UART 2 Transmit		ram_code3	VDDIO_UART	1.8	Bi-Dir
C59	I2S3_SCLK	I2S Audio Port 3 Clock			VDDIO_AUDIO_HV	3.3	Bidirectional
C60	I2S3_FS	I2S Audio Port 3 Left/Right Clock			VDDIO_AUDIO_HV	3.3	Bidirectional
C61	GPIO09	GPIO / Digital Mic Input Clock			VDDIO_AO_HV	3.3	Bi-Dir
C62	GND	GND					
C63	SYS_VIN_HV	System Voltage Input				9V-20V	Input
C64	SYS_VIN_HV					9V-20V	Input
C65	SYS_VIN_HV					9V-20V	Input
D1	SYS_VIN_HV					9V-20V	Input
D2	SYS_VIN_HV					9V-20V	Input
D3	SYS_VIN_HV					9V-20V	Input
D4	GND	GND					
D5	RGMII_RX_CTL	Ethernet Receive Control	Wake28		VDDIO_EQOS	1.8	Input
D6	SDCARD_D3	SD Card (or SDIO) Data 3			VDDIO_SDMMC1_HV	3.3	Bi-Dir
D7	GND	GND					
D8	I2S1_FS	I2S Audio Port 1 Left/Right Clock			VDDIO_AUDIO	1.8	Input
D9	PEX_L1_CLKREQ_N	PCIE 1 Clock Request	Wake54		VDDIO_PEX_CTL	1.8	Bi-Dir
D10	PEX_L0_RST_N	PCIe 0 Reset.			VDDIO_PEX_CTL	1.8	Output

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
D11	GND	GND					
D12	UPHY_RX11_P	UPHY Receive 11+					Input
D13	UPHY_RX11_N	UPHY Receive 11-					Input
D14	GND	GND					
D15	GND	GND					
D16	UPHY_RX7_P	UPHY Receive 7+					Input
D17	UPHY_RX7_N	UPHY Receive 7-					Input
D18	GND	GND					
D19	GND	GND					
D20	UPHY_RX3_P	UPHY Receive 3+					Input
D21	UPHY_RX3_N	UPHY Receive 3-					Input
D22	GND	GND					
D23	GND	GND					
D24	NVHS0_SLVS_RX0_P	PCIe/SLVS 0 Receive 0+			DVDDIO_NVHS0	1	Input
D25	NVHS0_SLVS_RX0_N	PCIe/SLVS 0 Receive 0-			DVDDIO_NVHS0	1	Input
D26	GND	GND					
D27	GND	GND					
D28	NVHS0_SLVS_RX4_P	PCIe/SLVS 0 Receive 4+			DVDDIO_NVHS0	1	Input
D29	NVHS0_SLVS_RX4_N	PCIe/SLVS 0 Receive 4-			DVDDIO_NVHS0	1	Input
D30	GND	GND					
D31	GND	GND					
D32	RSVD	-					
D33	RSVD	-					
D34	GND	GND					
D35	GND	GND					
D36	RSVD	-					
D37	RSVD	-					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
D38	GND	GND					
D39	GND	GND					
D40	MID3	Module ID 3					
D41	GND	GND					
D42	CSI5_D0_P	Camera, CSI 5 Data 0+			AVDD_CSI	1.2	Input
D43	CSI5_D0_N	Camera, CSI 5 Data 0–			AVDD_CSI	1.2	Input
D44	GND	GND					
D45	CSI5_D1_N	Camera, CSI 5 Data 1–			AVDD_CSI	1.2	Input
D46	CSI5_D1_P	Camera, CSI 5 Data 1+			AVDD_CSI	1.2	Input
D47	GND	GND					
D48	HDMI_DP1_TX2_N	DisplayPort 1 Lane 2– or HDMI Lane 0–			AVDDIO_HDMI_DP1	1	Output
D49	HDMI_DP1_TX2_P	DisplayPort 1 Lane 2+ or HDMI Lane 0+			AVDDIO_HDMI_DP1	1	Output
D50	GND	GND					
D51	HDMI_DP2_TX0_P	DisplayPort 2 Lane 0+ or HDMI Lane 2+			AVDDIO_HDMI_DP2	1	Output
D52	HDMI_DP2_TX0_N	DisplayPort 2 Lane 0– or HDMI Lane 2–			AVDDIO_HDMI_DP2	1	Output
D53	GND	GND					
D54	GPIO03	GPIO / DGPU Alert	Wake59		VDDIO_EDP	1.8	Bi-Dir
D55	SPI1_MOSI	SPI 1 Initiator Out / Target In			VDDIO_UART	1.8	Bi-Dir
D56	SPI3_MISO	SPI 3 Initiator In / Target Out			VDDIO_UART	1.8	Bi-Dir
D57	GND	GND					
D58	JTAG_TDO	JTAG Test Data Out			VDDIO_DEBUG	1.8	Output
D59	CAN0_DOUT	CAN 0 Transmit				3.3	
D60	SPI2_CS0_N	(JAX) SPI 2 Chip Select 0 / **(JAXi) Initiate IST**	Wake39		VDDIO_AO	1.8	Bi-Dir
D61	I2C4_CLK	General I2C 4 Clock			VDDIO_AO	1.8	Bi-Dir

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
D62	SPI2_MISO	(JAX) SPI 2 Initiator In / Target Out / **(JAXi) Safety MCU Communication**			VDDIO_AO	1.8	Bi-Dir
D63	GND	GND					
D64	SYS_VIN_HV	System Voltage Input				9V-20V	Input
D65	SYS_VIN_HV					9V-20V	Input
E1	SYS_VIN_HV					9V-20V	Input
E2	SYS_VIN_HV					9V-20V	Input
E3	GND	GND					
E4	I2S2_FS	I2S Audio Port 2 Left/Right Clock			VDDIO_CONN	1.8	Bidirectional
E5	RGMII_RD3	Ethernet Receive data bit 3			VDDIO_EQOS	1.8	Input
E6	RGMII_SMA_MDC	Ethernet Management Clock			VDDIO_EQOS	1.8	Output
E7	RGMII_SMA_MDIO	Ethernet Management Data	Wake17		VDDIO_EQOS	1.8	Bidirectional
E8	SDCARD_D0	SD Card (or SDIO) Data 0			VDDIO_SDMMC1_HV	3.3	Bi-Dir
E9	GND	GND					
E10	GPIO12	(JAX) GPIO (M2 Wake AP) / **(JAXi) Boot Chain Support**	Wake15		VDDIO_AUDIO	1.8	Bi-Dir
E11	PEX_L0_CLKREQ_N	PCIE 0 Clock Request.			VDDIO_PEX_CTL	1.8	Bi-Dir
E12	GND	GND					
E13	GND	GND					
E14	PEX_CLK0_N	PCIe 0 Reference Clock+			VDDIO_PEX_CLK	1.8	Output
E15	PEX_CLK0_P	PCIe 0 Reference Clock–			VDDIO_PEX_CLK	1.8	Output
E16	GND	GND					
E17	GND	GND					
E18	RSVD	-					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
E19	RSVD	-					
E20	GND	GND					
E21	GND	GND					
E22	PEX_CLK4_N	PCIe 4 Reference Clock					Output
E23	PEX_CLK4_P						Output
E24	GND	GND					
E25	GND	GND					
E26	UPHY_REFCLK1_N	UPHY Reference Clock 1- used when JAX is an Endpoint					Input
E27	UPHY_REFCLK1_P	UPHY Reference Clock 1+ used when JAX is an Endpoint					Input
E28	GND	GND					
E29	GND	GND					
E30	NVHS0_SLVS_REFCLK0_P	Reference Clock 0+ used when JAX is an Endpoint			DVDDIO_NVHS0	1	Input
E31	NVHS0_SLVS_REFCLK0_N	Reference Clock 0- used when JAX is an Endpoint			DVDDIO_NVHS0	1	Input
E32	GND	GND					
E33	GND	GND					
E34	RSVD	-					
E35	RSVD	-					
E36	GND	GND					
E37	GND	GND					
E38	CSI0_D1_N	Camera, CSI 0 Data 1–			AVDD_CSI	1.2	Input
E39	CSI0_D1_P	Camera, CSI 0 Data 1+			AVDD_CSI	1.2	Input
E40	GND	GND					
E41	CSI0_D0_N	Camera, CSI 0 Data 0–			AVDD_CSI	1.2	Input
E42	CSI0_D0_P	Camera, CSI 0 Data 0+			AVDD_CSI	1.2	Input

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
E43	GND	GND					
E44	CSI3_D0_N	Camera, CSI 3 Data 0–			AVDD_CSI	1.2	Input
E45	CSI3_D0_P	Camera, CSI 3 Data 0+			AVDD_CSI	1.2	Input
E46	GND	GND					
E47	CSI4_D1_P	Camera, CSI 4 Data 1+			AVDD_CSI	1.2	Input
E48	CSI4_D1_N	Camera, CSI 4 Data 1–			AVDD_CSI	1.2	Input
E49	GND	GND					
E50	HDMI_DP1_TX3_P	DisplayPort 1 Lane 3+ or HDMI Clk Lane+			AVDDIO_HDMI_DP1	1	Output
E51	HDMI_DP1_TX3_N	DisplayPort 1 Lane 3– or HDMI Clk Lane–			AVDDIO_HDMI_DP1	1	Output
E52	GND	GND					
E53	I2C3_DAT	General I2C 3 Data	Wake22		VDDIO_CAM	1.8	Bi-Dir
E54	FAN_TACH	Fan Tachometer signal	Wake51		VDDIO_CAM	1.8	Input
E55	SPI1_CS0_N	SPI 1 Chip Select 0	Wake45		VDDIO_UART	1.8	Bi-Dir
E56	SPI3_CS1_N	SPI 3 Chip Select 1	Wake58		VDDIO_UART	1.8	Bi-Dir
E57	GND_012	GND					
E58	JTAG_TMS	JTAG Test Mode Select			VDDIO_DEBUG	1.8	Input
E59	GPIO06	GPIO			VDDIO_AO_HV	3.3	Bi-Dir
E60	I2C4_DAT	General I2C 4 Data	Wake21		VDDIO_AO	1.8	Bi-Dir
E61	SPI2_CLK	(JAX) SPI 2 Clock / **(JAXi) Safety MCU Communication**			VDDIO_AO	1.8	Bi-Dir
E62	GND	GND					
E63	SYS_VIN_HV	System Voltage Input				9V-20V	Input
E64	SYS_VIN_HV					9V-20V	Input
E65	SYS_VIN_HV					9V-20V	Input
F1	SYS_VIN_HV					9V-20V	Input
F2	SYS_VIN_HV					9V-20V	Input

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
F3	SYS_VIN_HV					9V-20V	Input
F4	GND	GND					
F5	I2S2_DOUT	I2S Audio Port 2 Data Out			VDDIO_CONN	1.8	Output
F6	I2S2_DIN	I2S Audio Port 2 Data In			VDDIO_CONN	1.8	Input
F7	GND	GND					
F8	SDCARD_D1	SD Card (or SDIO) Data 1	Wake3		VDDIO_SDMMC1_HV	3.3	Bi-Dir
F9	GPIO16	GPIO (Camera 1 Reset) / Digital Speaker Output Data			VDDIO_AUDIO	1.8	Bi-Dir
F10	GPIO15	GPIO (Camera 1 Powerdown) / Digital Speaker Output Clock			VDDIO_AUDIO	1.8	Bi-Dir
F11	GND	GND					
F12	USB0_P	USB 2.0 Port 0 Data+			AVDD_USB	3.3	Bi-Dir
F13	USB0_N	USB 2.0 Port 0 Data–			AVDD_USB	3.3	Bi-Dir
F14	GND	GND					
F15	GND	GND					
F16	PEX_CLK1_P	PCIe 1 Reference Clock–			VDDIO_PEX_CLK	1.8	Output
F17	PEX_CLK1_N	PCIe 1 Reference Clock+			VDDIO_PEX_CLK	1.8	Output
F18	GND	GND					
F19	GND	GND					
F20	PEX_CLK3_P	PCIe 3 Reference Clock–			VDDIO_PEX_CLK	1.8	Output
F21	PEX_CLK3_N	PCIe 3 Reference Clock+			VDDIO_PEX_CLK	1.8	Output
F22	GND	GND					
F23	GND	GND					
F24	PEX_CLK5_P	PCIe 5 Reference Clock– when JAX is Root Port. Unused when JAX used as Endpoint.			VDDIO_PEX_CLK2	1.8	Output

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
F25	PEX_CLK5_N	PCIe 5 Reference Clock+ when JAX is Root Port. Unused when JAX used as Endpoint.			VDDIO_PEX_CLK2	1.8	Output
F26	GND	GND					
F27	GND	GND					
F28	RSVD	-					
F29	RSVD	-					
F30	GND	GND					
F31	GND	GND					
F32	RSVD	-					
F33	RSVD	-					
F34	GND	GND					
F35	GND	GND					
F36	RSVD	-					
F37	RSVD	-					
F38	GND	GND					
F39	GND	GND					
F40	MID2	Module ID 2					
F41	GND	GND					
F42	CSI0_CLK_N	Camera, CSI 0 Clock–			AVDD_CSI	1.2	Input
F43	CSI0_CLK_P	Camera, CSI 0 Clock+			AVDD_CSI	1.2	Input
F44	GND	GND					
F45	CSI3_CLK_N	Camera, CSI 3 Clock–			AVDD_CSI	1.2	Input
F46	CSI3_CLK_P	Camera, CSI 3 Clock+			AVDD_CSI	1.2	Input
F47	GND	GND					
F48	CSI4_CLK_P	Camera CSI 4 Clock+			AVDD_CSI	1.2	Input
F49	CSI4_CLK_N	Camera, CSI 4 Clock–			AVDD_CSI	1.2	Input
F50	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
F51	DP0_AUX_CH_N	Display Port 0 Aux– or HDMI DDC SDA			VDDIO_EDP	1.8	Bi-Dir
F52	DP0_AUX_CH_P	Display Port 0 Aux+ or HDMI DDC SCL			VDDIO_EDP	1.8	Bi-Dir
F53	I2C3_CLK	General I2C 3 Clock			VDDIO_CAM	1.8	Bi-Dir
F54	GPIO22	GPIO	Wake61		VDDIO_UART	1.8	Bi-Dir
F55	SPI3_CLK	SPI 3 Clock	Wake44		VDDIO_UART	1.8	Bi-Dir
F56	GPIO36	GPIO			VDDIO_EDP	1.8	Bi-Dir
F57	GND	GND					
F58	CAN0_DIN	CAN 0 Receive	IO	de-glitch		3.3	
F59	GPIO07	GPIO	Wake46		VDDIO_AO_HV	3.3	Bi-Dir
F60	SPI2_MOSI	(JAX) SPI 2 Initiator Out / Target In / **(JAXi) IST Complete**			VDDIO_AO	1.8	Bi-Dir
F61	VCOMP_ALERT_N	Voltage Comparator Alert	Wake26		VDDIO_SYS	1.8	Input
F62	GND	GND					
F63	SYS_VIN_HV	System Voltage Input				9V-20V	Input
F64	SYS_VIN_HV					9V-20V	Input
F65	SYS_VIN_HV					9V-20V	Input
G1	SYS_VIN_HV					9V-20V	Input
G2	SYS_VIN_HV					9V-20V	Input
G3	GND	GND					
G4	I2S2_CLK	I2S Audio Port 2 Clock			VDDIO_CONN	1.8	Bidirectional
G5	RGMII_TD1	Ethernet Transmit data bit 1			VDDIO_EQOS	1.8	Output
G6	RGMII_TD3	Ethernet Transmit data bit 3			VDDIO_EQOS	1.8	Output
G7	GPIO13	GPIO			VDDIO_AUDIO	1.8	Bi-Dir
G8	PEX_L4_CLKREQ_N	PCIe 4 Clock Request.				1.8	Input
G9	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
G10	USB3_N	USB 2.0, Port 3 Data–			AVDD_USB	3.3	Bi-Dir
G11	USB3_P	USB 2.0, Port 3 Data+			AVDD_USB	3.3	Bi-Dir
G12	GND	GND					
G13	GND	GND					
G14	UPHY_TX9_N	UPHY Transmit 9-					Output
G15	UPHY_TX9_P	UPHY Transmit 9+					Output
G16	GND	GND					
G17	GND	GND					
G18	UPHY_TX5_N	UPHY Transmit 5-					Output
G19	UPHY_TX5_P	UPHY Transmit 5+					Output
G20	GND	GND					
G21	GND	GND					
G22	UPHY_TX1_N	UPHY Transmit 1-					Output
G23	UPHY_TX1_P	UPHY Transmit 1+					Output
G24	GND	GND					
G25	GND	GND					
G26	NVHS0_TX2_N	PCIe/SLVS 0 Transmit 2-			DVDDIO_NVHS0	1	Output
G27	NVHS0_TX2_P	PCIe/SLVS 0 Transmit 2+			DVDDIO_NVHS0	1	Output
G28	GND	GND					
G29	GND	GND					
G30	NVHS0_TX6_N	PCIe/SLVS 0 Transmit 6-			DVDDIO_NVHS0	1	Output
G31	NVHS0_TX6_P	PCIe/SLVS 0 Transmit 6+			DVDDIO_NVHS0	1	Output

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
G32	GND	GND					
G33	GND	GND					
G34	RSVD	-					
G35	RSVD	-					
G36	GND	GND					
G37	GND	GND					
G38	RSVD	-					
G39	RSVD	-					
G40	GND	GND					
G41	CSI1_D0_P	Camera, CSI 1 Data 0+			AVDD_CSI	1.2	Input
G42	CSI1_D0_N	Camera, CSI 1 Data 0–			AVDD_CSI	1.2	Input
G43	GND	GND					
G44	CSI3_D1_P	Camera, CSI 3 Data 1+			AVDD_CSI	1.2	Input
G45	CSI3_D1_N	Camera, CSI 3 Data 1–			AVDD_CSI	1.2	Input
G46	GND	GND					
G47	CSI4_D0_N	Camera, CSI 4 Data 0–			AVDD_CSI	1.2	Input
G48	CSI4_D0_P	Camera, CSI 4 Data 0+			AVDD_CSI	1.2	Input
G49	GND	GND					
G50	HDMI_DP0_TX1_N	DisplayPort 0 Lane 1– or HDMI Lane 1–			AVDDIO_HDMI_DP0	1	Output
G51	HDMI_DP0_TX1_P	DisplayPort 0 Lane 1+or HDMI Lane 1+			AVDDIO_HDMI_DP0	1	Output
G52	GND	GND					
G53	DP2_AUX_CH_P	Display Port 2 Aux+ or HDMI DDC SCL			VDDIO_EDP	1.8	Bi-Dir
G54	DP2_AUX_CH_N	Display Port 2 Aux– or HDMI DDC SDA			VDDIO_EDP	1.8	Bi-Dir
G55	GPIO23	GPIO	Wake62		VDDIO_UART	1.8	Bi-Dir
G56	SPI3_MOSI	SPI 3 Initiator Out / Target In			VDDIO_UART	1.8	Bi-Dir
G57	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
G58	UART2_RTS	UART 2 Request to Send		ram_code2	VDDIO_UART	1.8	Bi-Dir
G59	RSVD	(JAX) Reserved / **(JAXi) TEMP_THERM_N - TMP451 Shutdown**					
G60	NVDBG_SEL	NVIDIA Debug Select	Wake14		VDDIO_DEBUG	1.8	Input
G61	JTAG_TRST_N	JTAG Test Reset			VDDIO_DEBUG	1.8	Input
G62	GND	GND					
G63	SYS_VIN_HV	System Voltage Input				9V-20V	Input
G64	SYS_VIN_HV					9V-20V	Input
G65	SYS_VIN_HV					9V-20V	Input
H1	SYS_VIN_HV					9V-20V	Input
H2	SYS_VIN_HV					9V-20V	Input
H3	SYS_VIN_HV					9V-20V	Input
H4	GND	GND					
H5	ENET_RST_N	Ethernet Reset			VDDIO_CONN	1.8	
H6	RGMII_RD2	Ethernet Receive data bit 2			VDDIO_EQOS	1.8	Input
H7	GND	GND					
H8	I2S1_SDIN	I2S Audio Port 1 Data In			VDDIO_AUDIO	1.8	Output
H9	MCLK01	Audio Codec Initiator Clock			VDDIO_AUDIO	1.8	Output
H10	PEX_L5_RST_N	PCIe 5 Reset. Output when JAX is Root Port. Input when JAX is Endpoint.			VDDIO_PEX_CTL_2	1.8	Output
H11	GND	GND					
H12	UPHY_TX11_P	UPHY Transmit 11+					Output
H13	UPHY_TX11_N	UPHY Transmit 11-					Output
H14	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
H15	GND	GND					
H16	UPHY_TX7_P	UPHY Transmit 7+					Output
H17	UPHY_TX7_N	UPHY Transmit 7-					Output
H18	GND	GND					
H19	GND	GND					
H20	UPHY_TX3_P	UPHY Transmit 3+					Output
H21	UPHY_TX3_N	UPHY Transmit 3-					Output
H22	GND	GND					
H23	GND	GND					
H24	NVHS0_TX0_P	PCIe/SLVS 0 Transmit 0+			DVDDIO_NVHS0	1	Output
H25	NVHS0_TX0_N	PCIe/SLVS 0 Transmit 0-			DVDDIO_NVHS0	1	Output
H26	GND	GND					
H27	GND	GND					
H28	NVHS0_TX4_P	PCIe/SLVS 0 Transmit 4+			DVDDIO_NVHS0	1	Output
H29	NVHS0_TX4_N	PCIe/SLVS 0 Transmit 4-			DVDDIO_NVHS0	1	Output
H30	GND	GND					
H31	GND	GND					
H32	RSVD	-					
H33	RSVD	-					
H34	GND	GND					
H35	GND	GND					
H36	RSVD	-					
H37	RSVD	-					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
H38	GND	GND					
H39	GND	GND					
H40	MID1	Module ID 1					
H41	GND	GND					
H42	CSI1_CLK_N	Camera, CSI 1 Clock–			AVDD_CSI	1.2	Input
H43	CSI1_CLK_P	Camera, CSI 1 Clock+			AVDD_CSI	1.2	Input
H44	GND	GND					
H45	CSI6_D1_N	Camera, CSI_6 Data 1–			AVDD_CSI	1.2	Input
H46	CSI6_D1_P	Camera, CSI_6 Data 1+			AVDD_CSI	1.2	Input
H47	GND	GND					
H48	HDMI_DP0_TX0_N	DisplayPort 0 Lane 0– or HDMI Lane 2–			AVDDIO_HDMI_DP0	1	Output
H49	HDMI_DP0_TX0_P	DisplayPort 0 Lane 0+ or HDMI Lane 2+			AVDDIO_HDMI_DP0	1	Output
H50	GND	GND					
H51	GPIO26	GPIO			VDDIO_EDP	1.8	Bi-Dir
H52	GPIO27	GPIO	Wake4		VDDIO_EDP	1.8	Bi-Dir
H53	MCLK03	Camera 1 Initiator Clock			VDDIO_CAM	1.8	Output
H54	UART1_CTS	UART 1 Clear to Send	Wake33		VDDIO_CAM	1.8	Bi-Dir
H55	MCLK04	Camera 2 Initiator Clock			VDDIO_CAM	1.8	Output
H56	GND	GND					
H57	UART5_CTS	UART 5 Clear to Send	Wake53		VDDIO_UART	1.8	Bi-Dir
H58	UART5_RX	UART 5 Receive			VDDIO_UART	1.8	Bi-Dir
H59	NVJTAG_SEL	NVIDIA JTAG Select			VDDIO_DEBUG	1.8	Input
H60	GPIO31	(JAX) GPIO / **(JAXi) GPIO31_SAFESTATE - Nsafe for 3LSS**	Wake25		VDDIO_SYS	1.8	Bi-Dir
H61	CAN1_DOUT	CAN 1 Transmit				3.3	

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
H62	UART3_TX_DEBUG	Debug UART Transmit			VDDIO_AO	1.8	Output
H63	GND	GND					
H64	SYS_VIN_HV	System Voltage Input				9V-20V	Input
H65	SYS_VIN_HV					9V-20V	Input
J1	SYS_VIN_HV					9V-20V	Input
J2	SYS_VIN_HV					9V-20V	Input
J3	GND	GND					
J4	GPIO01	GPIO	Wake30	rcm_2	VDDIO_CONN	1.8	Bi-Dir
J5	ENET_INT	Ethernet Interrupt	Wake20		VDDIO_CONN	1.8	
J6	RGMII_TD0	Ethernet Transmit data bit 0			VDDIO_EQOS	1.8	Output
J7	RGMII_TD2	Ethernet Transmit data bit 2			VDDIO_EQOS	1.8	Output
J8	GND	GND					
J9	PEX_L4_RST_N	PCIe 4 Reset.				1.8	Output
J10	PEX_L3_CLKREQ_N	PCIE 3 Clock Request	Wake65		VDDIO_PEX_CTL	1.8	Bi-Dir
J11	RSVD	-					
J12	GND	GND					
J13	GND	GND					
J14	UPHY_TX8_P	UPHY Transmit 8+					Output
J15	UPHY_TX8_N	UPHY Transmit 8-					Output
J16	GND	GND					
J17	GND	GND					
J18	UPHY_TX4_P	UPHY Transmit 4+					Output
J19	UPHY_TX4_N	UPHY Transmit 4-					Output

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
J20	GND	GND					
J21	GND	GND					
J22	UPHY_TX0_P	UPHY Transmit 0+					Output
J23	UPHY_TX0_N	UPHY Transmit 0-					Output
J24	GND	GND					
J25	GND	GND					
J26	NVHS0_TX3_P	PCIe/SLVS 0 Transmit 3+			DVDDIO_NVHS0	1	Output
J27	NVHS0_TX3_N	PCIe/SLVS 0 Transmit 3-			DVDDIO_NVHS0	1	Output
J28	GND	GND					
J29	GND	GND					
J30	NVHS0_TX7_P	PCIe/SLVS 0 Transmit 7+			DVDDIO_NVHS0	1	Output
J31	NVHS0_TX7_N	PCIe/SLVS 0 Transmit 7-			DVDDIO_NVHS0	1	Output
J32	GND	GND					
J33	GND	GND					
J34	RSVD	-					
J35	RSVD	-					
J36	GND	GND					
J37	GND	GND					
J38	RSVD	-					
J39	RSVD	-					
J40	GND	GND					
J41	CSI1_D1_P	Camera, CSI 1 Data 1+			AVDD_CSI	1.2	Input
J42	CSI1_D1_N	Camera, CSI 1 Data 1–			AVDD_CSI	1.2	Input
J43	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
J44	CSI6_CLK_P	Camera, CSI_6 Clock+			AVDD_CSI	1.2	Input
J45	CSI6_CLK_N	Camera, CSI 5 Clock–			AVDD_CSI	1.2	Input
J46	GND	GND					
J47	HDMI_DP0_TX2_P	DisplayPort 0 Lane 2+ or HDMI Lane 0+			AVDDIO_HDMI_DP0	1	Output
J48	HDMI_DP0_TX2_N	DisplayPort 0 Lane 2– or HDMI Lane 0–			AVDDIO_HDMI_DP0	1	Output
J49	GND	GND					
J50	HDMI_CEC	HDMI CEC	Wake70		VDDIO_EDP	1.8	Bi-Dir
J51	GPIO24	GPIO	Wake66		VDDIO_EDP	1.8	Bi-Dir
J52	DP1_AUX_CH_P	Display Port 1 Aux+ or HDMI DDC SCL			VDDIO_EDP	1.8	Bi-Dir
J53	DP1_AUX_CH_N	Display Port 1 Aux– or HDMI DDC SDA			VDDIO_EDP	1.8	Bi-Dir
J54	MCLK02	Camera 0 Initiator Clock			VDDIO_CAM	1.8	Output
J55	GPIO32	GPIO	Wake34		VDDIO_CAM	1.8	Bi-Dir
J56	GND	GND					
J57	SPI1_CLK	SPI 1 Clock			VDDIO_UART	1.8	Bi-Dir
J58	UART5_TX	UART 5 Transmit		ram_code1	VDDIO_UART	1.8	Bi-Dir
J59	I2S3_DIN	I2S Audio Port 3 Data In			VDDIO_AUDIO_HV	3.3	Bidirectional
J60	STANDBY_ACK_N	Standby Acknowledge			VDDIO_SYS	1.8	Output
J61	I2C2_CLK	General I2C 2 Clock			VDDIO_AO	1.8	Bi-Dir
J62	GND	GND					
J63	SYS_VIN_HV	System Voltage Input				9V-20V	Input
J64	SYS_VIN_HV					9V-20V	Input
J65	SYS_VIN_HV					9V-20V	Input
K3	SYS_VIN_HV					9V-20V	Input
K4	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
K5	I2C1_CLK	General I2C 1 Clock			VDDIO_CONN	1.8	
K6	RGMII_RD1	Ethernet Receive data bit 1			VDDIO_EQOS	1.8	Input
K7	RGMII_TX_CTL	Ethernet Transmit Control			VDDIO_EQOS	1.8	Output
K8	GND	GND					
K9	PEX_L3_RST_N	PCIe 3 Reset			VDDIO_PEX_CTL	1.8	Output
K10	RSVD	-					
K11	GND	GND					
K12	UPHY_TX10_N	UPHY Transmit 10-					Output
K13	UPHY_TX10_P	UPHY Transmit 10+					Output
K14	GND	GND					
K15	GND	GND					
K16	UPHY_TX6_N	UPHY Transmit 6-					Output
K17	UPHY_TX6_P	UPHY Transmit 6+					Output
K18	GND	GND					
K19	GND	GND					
K20	UPHY_TX2_N	UPHY Transmit 2-					Output
K21	UPHY_TX2_P	UPHY Transmit 2+					Output
K22	GND	GND					
K23	GND	GND					
K24	NVHS0_TX1_N	PCIe/SLVS 0 Transmit 1-			DVDDIO_NVHS0	1	Output
K25	NVHS0_TX1_P	PCIe/SLVS 0 Transmit 1+			DVDDIO_NVHS0	1	Output
K26	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
K27	GND	GND					
K28	NVHS0_TX5_N	PCIe/SLVS 0 Transmit 5-			DVDDIO_NVHS0	1	Output
K29	NVHS0_TX5_P	PCIe/SLVS 0 Transmit 5+			DVDDIO_NVHS0	1	Output
K30	GND	GND					
K31	GND	GND					
K32	RSVD	-					
K33	RSVD	-					
K34	GND	GND					
K35	GND	GND					
K36	RSVD	-					
K37	RSVD	-					
K38	GND	GND					
K39	GND	GND					
K40	MID0	Module ID 0					
K41	GND	GND					
K42	GND	GND					
K43	CSI6_D0_N	Camera, CSI_6 Data 0–			AVDD_CSI	1.2	Input
K44	CSI6_D0_P	Camera, CSI_6 Data 0+			AVDD_CSI	1.2	Input
K45	GND	GND					
K46	HDMI_DP0_TX3_P	DisplayPort 0 Lane 3+ or HDMI Clk Lane+			AVDDIO_HDMI_DP0	1	Output
K47	HDMI_DP0_TX3_N	DisplayPort 0 Lane 3– or HDMI Clk Lane–			AVDDIO_HDMI_DP0	1	Output
K48	GND	GND					
K49	GPIO25	GPIO (SAR TOUT)			VDDIO_EDP	1.8	Bi-Dir
K50	DP2_HPD	Display Port/HDMI 2 Hot Plug Detect	Wake71		VDDIO_EDP	1.8	Input
K51	DP1_HPD	Display Port/HDMI 1 Hot Plug Detect	Wake63		VDDIO_EDP	1.8	Input

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
K52	DP0_HPD	Display Port/HDMI 0 Hot Plug Detect	Wake60		VDDIO_EDP	1.8	Input
K53	UART1_TX	UART 1 Transmit		boot_sel 2	VDDIO_CAM	1.8	Bi-Dir
K54	UART1_RX	UART 1 Receive			VDDIO_CAM	1.8	Bi-Dir
K55	GND	GND					
K56	GPIO19	GPIO			VDDIO_CAM	1.8	Bi-Dir
K57	PWM01	PWM 1			VDDIO_CAM	1.8	Output
K58	UART5_RTS	UART 5 Request to Send		ram_code0	VDDIO_UART	1.8	Bi-Dir
K59	I2S3_DOUT	I2S Audio Port 3 Data Out			VDDIO_AUDIO_HV	3.3	Bidirectional
K60	UART3_RX_DEBUG	Debug UART Receive			VDDIO_AO	1.8	Input
K61	I2C2_DAT	General I2C 2 Data	Wake41		VDDIO_AO	1.8	Bi-Dir
K62	FAN_PWM	Fan Pulse Width Modulation signal			VDDIO_AO	1.8	Output
K63	GND	GND					
L3	GND	GND					
L4	UART4_RTS	GPIO (Note: UART4 pins do not support UART functionality)		boot_sel 0	VDDIO_CONN	1.8	Output
L5	UART4_TX	GPIO (Note: UART4 pins do not support UART functionality)		boot_sel 1	VDDIO_CONN	1.8	Output
L6	GPIO02	GPIO	Wake8		VDDIO_CONN	1.8	Bi-Dir
L7	GND	GND					
L8	I2C1_DAT	General I2C 1 Data	Wake31		VDDIO_CONN	1.8	
L9	GPIO28	GPIO	Wake69		VDDIO_CONN	1.8	Bi-Dir
L10	FORCE_RECOVERY_N	Force Recovery strap pin	Wake67	rcm_0	VDDIO_CONN	1.8	Input
L11	STANDBY_REQ_N	Standby Request	Wake68	rcm_1	VDDIO_CONN	1.8	Input
L12	GND	GND					
L13	GND	GND					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
L14	I2S1_CLK	I2S Audio Port 1 Clock			VDDIO_AUDIO	1.8	Bi-Dir
L15	GPIO14	(JAX) GPIO (M2 Enable) / **(JAXi) TEMP_ALRT_N - TMP451 Alert**			VDDIO_AUDIO	1.8	Bi-Dir
L16	GND	GND					
L17	GND	GND					
L18	RSVD	-					
L19	RSVD	-					
L20	GND	GND					
L21	GND	GND					
L22	SYS_VIN_MV	5V Input				5V	Input
L23	SYS_VIN_MV					5V	Input
L24	GND	GND					
L25	GND	GND					
L26	SYS_VIN_MV	5V Input				5V	Input
L27	SYS_VIN_MV					5V	Input
L28	GND	GND					
L29	GND	GND					
L30	SYS_VIN_MV	5V Input				5V	Input
L31	SYS_VIN_MV					5V	Input
L32	GND	GND					
L33	GND	GND					
L34	SYS_VIN_MV	5V Input				5V	Input
L35	SYS_VIN_MV					5V	Input
L36	GND	GND					
L37	GND	GND					
L38	SYS_VIN_MV	5V Input				5V	Input
L39	SYS_VIN_MV					5V	Input

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
L40	GND	GND					
L41	RSVD	-					
L42	RSVD	-					
L43	GND	GND					
L44	RSVD	-					
L45	RSVD	-					
L46	GND	GND					
L47	RSVD	-					
L48	UART4_RX	Reserved – Must be pulled to GND through 10kΩ resistor.(Note: UART4 pins do not support UART functionality; see *NVIDIA Jetson OEM Product Design Guide*)			VDDIO_CONN	1.8	Input
L49	UART4_CTS	GPIO (Note: UART4 pins do not support UART functionality)	Wake7		VDDIO_CONN	1.8	Bidirectional
L50	GPIO35	GPIO			VDDIO_CONN	1.8	Bi-Dir
L51	UART1_RTS	UART 1 Request to Send		ufs_sel	VDDIO_CAM	1.8	Bi-Dir
L52	OVERTEMP_N	Over temperature Alert	Wake64		VDDIO_EDP	1.8	
L53	VCC_RTC	Real-Time-Clock (accuracy = 2 seconds/day). Optionally used to provide back-up power for RTC. Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.					
L54	MODULE_POWER_ON	Module Power On					Input
L55	VDDIN_PWR_BAD_N	Power Bad. Carrier board indication to the module that the VIN power is not valid. Carrier board should de-assert this (drive high) only when VIN has reached its required voltage level and is stable. This prevents the module from powering up until the VIN power is stable.					Input
L56	TEMP_ALERT_N	Temperature Alert					

Ball	Signal	Usage/Description	Wake	Strap	Group	Voltage	Direction
L57	MCLK05	Camera 2 Initiator Clock			VDDIO_CAM	1.8	Output
L58	PERIPHERAL_RESET_N	Peripheral Reset. Driven from carrier board to force reset of module, eMMC, and QSPI (not PMIC).					
L59	RSVD	-					
L60	SYS_RESET_N	System Reset: Connected to NRST_IO of PMIC. Bidirectional reset driven from PMIC to carrier board for devices requiring full system reset. Can also be driven from carrier board to module to initiate full system reset (including PMIC) (i.e. From RESET button). A pull-up is present on module.			VDDIO_SYS	1.8	Bi-Dir
L61	POWER_BTN_N	Power Button. Used to initiate a system power-on & to resume from SC7.	Wake29		VDDIO_SYS	1.8	Input
L62	CARRIER_POWER_ON	Carrier Power On. Used as part of the power up sequence. The module asserts this signal when it is safe for the carrier board to power up.				3.3V	Output
L63	PRSNT1						

4 Physical / Electrical Characteristics

4.1 Absolute Maximum Ratings

The absolute maximum ratings describe stress conditions. These parameters do not set minimum and maximum operating conditions that will be tolerated over extended periods of time. If the device is exposed to these parameters for extended periods of time, no guarantee is made and device reliability may be affected. It is not recommended to operate a JAX series module under these conditions, recommended operating conditions are provided in the following section.

Symbol	Parameter	Min	Max	Unit	Notes
VIN	SYS_VIN_HV	-0.5	22.5	V	
	SYS_VIN_MV	-0.5	6.0	V	
	VCC_RTC	-0.3	6.0	V	
IDD_{MAX}	VIN Imax (SYS_VIN_HV)		5.4	A	Software limited. IDD_{MAX} (HV/MV current) reflects EDPp based on a 6uS moving window. 5.4A is for VIN(20V) on SYS_VIN_HV. 6.0A is for VIN (5V) on SYS_VIN_MV. Actual IDD_{MAX} is dependent on VIN (VIN_{MIN})
	VIN Imax (SYS_VIN_MV)		6.0	A	
V_{M_PIN}	Voltage applied to any powered I/O pin	-0.5	VDD + 0.5	V	
	DD pads configured as open drain	-0.5	3.63	V	pad's output-driver must be set to open-drain mode
T_{TTP}	Operating Temperature: measured on Thermal Transfer Plate	(JAX) -25 **(JAXi) -40**	(JAX) 80 **(JAXi) 85**	°C	**(JAXi) 24x7 operation for 10-years**
T_{STG}	Storage Temperature	(JAX) -25 **(JAXi) -40**	(JAX) 80 **(JAXi) 85**	°C	

4.2 Recommended Operating Conditions

The parameters listed in following table are specific to a temperature range and operating voltage. Operating a JAX series module beyond these parameters is not recommended. Exceeding these conditions for extended periods may adversely affect device reliability.

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD_{DC}	SYS_VIN_HV	9.0		20.0	V	
	SYS_VIN_MV	4.75		5.25	V	

Symbol	Parameter	Min	Typical	Max	Unit	Notes
	VCC_RTC					
	Input	1.65		5.5	V	Powering PMIC BBATT
	Output	2.5		3.5	V	To charge supercap/battery

4.3 Digital Logic

Voltages less than the minimum stated value can be interpreted as an undefined state or logic level low which may result in unreliable operation . Voltages exceeding the maximum value can damage and/or adversely affect device reliability.

Table 11 CMOS Pin Type DC Characteristics

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.70 x VDD	0.5 + VDD	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.75 x VDD	---	V

Table 12 Open Drain Pin Type DC Characteristics

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	3.63	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V
	I2C Output Low Voltage (I_{OL} = 3.3mA)	---	0.3 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	---	V

4.4 Environmental & Mechanical Screening

Module performance was assessed against a series of industry standard tests designed to evaluate robustness and estimate the failure rate of an electronic assembly in the environment in which it will be used. Mean Time Between Failures (MTBF) calculations are produced in the design phase to predict a product's future reliability in the field.

Jetson JAXi modules are manufactured according to IPC-A-610 class 3 High Performance Electronic Product standards.

Table 13 JAX Testing

Test	Test Conditions	Reference Standard
Board-level Temperature Cycling	-40°C to 105°C, 750 cycles, non-operational	JESD22-A104, IPC9701
System-level Temperature Cycling	-20°C to 70°C, 100 cycles, non-operational	ISO 16750-4, IEC60068-2-14
Temperature Humidity Biased	85°C / 85% RH, 2000 hours, power ON	JESD22-A101
Temperature Humidity Cycling	-10°C to 65°C, 95% RH, 10 cyc / 240 hours, non-operational	IEC60068-2-38
Low Temperature Endurance	-20°C, 24 hours, operational	IEC60068-2-1
High Temperature Endurance	40°C, 168 hours, operational	IEC60068-2-2
Low Temperature Storage	-40°C 72 hours, non-operational	IEC60068-2-1
High Temperature Storage	85°C, 96 hours, non-operational	IEC60068-2-2
Damp Heat Steady State	65°C, 95% RH, 24 hours, non-condensing	IEC60068-2-78
Connector Insertion Cycling	Insert and withdraw connector, 30 cycles	EIA-364
Sine Vibration – 5G 2 sweeps	10-500 Hz, 5 Grms, 3 axes, 2 sweeps/axis, non-operational	IEC60068-2-6
Random Vibration – 5G	10-500 Hz, 5 Grms, 8 hours/axis, non-operational	IEC60068-2-64
Mechanical Shock – 340G	340G, 2 msec, half sine, 6 shocks/axis, 3 axes, non-operational	JESD22-B110
Free Fall Drop	1m concrete, 6 faces, 1 drop/face, non-operational	NV Standard
TTP Assembly	TTP assembly & disassembly, 6 times	NV Standard

Test	Test Conditions	Reference Standard
Altitude	0 to 16k feet, 2k feet/min, operational 0 to 40k feet, 2k feet/min, non-operational	ASTMD6653
Burn In	40°C, 1000 hours, operational	NV Standard
Hard Boot	ON for 90 sec, OFF for 20 sec 2500 cycles at 25°C, 2500 cycles at -20°C, 2500 cycles at 45°C	NV Standard
MTBF / Failure Rate: 1,634,290 Hours / 612 FIT	Controlled Environment (GB), T = 35°C, UCL = 90%	Telcordia SR-332, ISSUE 3, Parts Count (Method I)
MTBF / Failure Rate: 1,018,309 Hours / 982 FIT	Uncontrolled Environment (GF) T = 35°C, UCL = 90%	Telcordia SR-332, ISSUE 3, Parts Count (Method I)
MTBF / Failure Rate: 569,490 Hours / 1756 FIT	Ground Mobile (GM)T = 35°C, UCL = 90%	Telcordia SR-332, ISSUE 3, Parts Count (Method I)

Table 14 JAXi Testing

Test	Test Conditions	Reference Standard
Board-level Temperature Cycling	-40°C to 105°C, 43 min/cycle, FCT/EC/DPA, non-operational	JESD22-A104 TCT
Board-level Power Cycling	35°C to 130°C, 15 min/cycle, FCT/DPA, heater, non-operational	OPSQA0111 - BLPC
Temperature Humidity Biased	85°C / 85% RH, power ON	JESD22-A101
Random Vibration	10-1000 Hz, 3 G_{rms}, 3-axis, FCT, non-operational	IEC60068-2-64
	10-500 Hz, 5 G_{rms}, 3-axis, FCT, operational	
Mechanical Shock	Half Sine,140G, 2 msec, 3-axis, FCT/DPA, extend to 340G, non-operational	JESD22-B110
	Half Sine, 50G, 11 msec, 3-axis, operational	IEC 600068 2-27
Free Fall Drop	1m on concrete, 6 faces, FCT/DPA, non-operational	NV Standard
Connector Insertion with Base Board	Mount/un-mount from baseboard 30x, FCT/DPA, non-operational	NV Standard

Test	Test Conditions	Reference Standard
Low Temperature Storage	-40°C, 72 hours, non-operational	IEC60068-2-1
High Temperature Storage	85°C, 96 hours, non-operational	IEC60068-2-2
Low Temperature Endurance	-40°C, 96 hours, FCT, operational	IEC60068-2-1
High Temperature Endurance	60°C, 1500 hours, FCT, operational	IEC60068-2-2
Temperature Humidity Cycling	-10°C to 25°C to 65°C, 95% RH, non-operational	IEC60068-2-38
Damp Heat Steady State	60°C, 95% RH (+/- 3%), non-condensing, operational	IEC60068-2-78
Sine Vibration	10-500 Hz, 5 G_{rms}, 3 axes, 2 sweeps/axis, FCT, Visual, operational	IEC60068-2-6
Altitude	0 to 16k feet, 2k feet/min altitude change, operational 0 to 40k feet, 2k feet/min altitude change, non-operational	ASTMD6653
Hard Boot (Room Temp)	ON for 150 sec, OFF for 30 sec 37,800 cycles at 25°C, operational	NV Standard
Hard Boot (Low Temp)	ON for 150 sec, OFF for 30 sec 10,800 cycles at -40°C, operational	NV Standard
Hard Boot (High Temp)	ON for 90 sec, OFF for 20 sec 5,400 cycles at 85°C, operational	NV Standard
MTBF: 1,446,862 Hours	Controlled Environment (GB), T = 35°C, UCL = 90%	Telcordia (TelC4) SR-332, ISSUE 4, Calculation Methodology: Parts Count (Method I), Quality level: II
MTBF: 1,101,528 Hours	Uncontrolled Environment (GF) T = 35°C, UCL = 90%	Telcordia (TelC4) SR-332, ISSUE 4, Calculation Methodology: Parts Count (Method I), Quality level: II

4.5 Package Drawings and Dimensions

Total module height includes the module PCB, thermal transfer plate (TTP), and bottom cover. Implementations vary, NVIDIA does not specify the height of a complete cooling solution; refer to the Thermal Design Guide for additional information/ guidance on designing a cooling solution that meets system needs.

Module Dimensions/Weight:

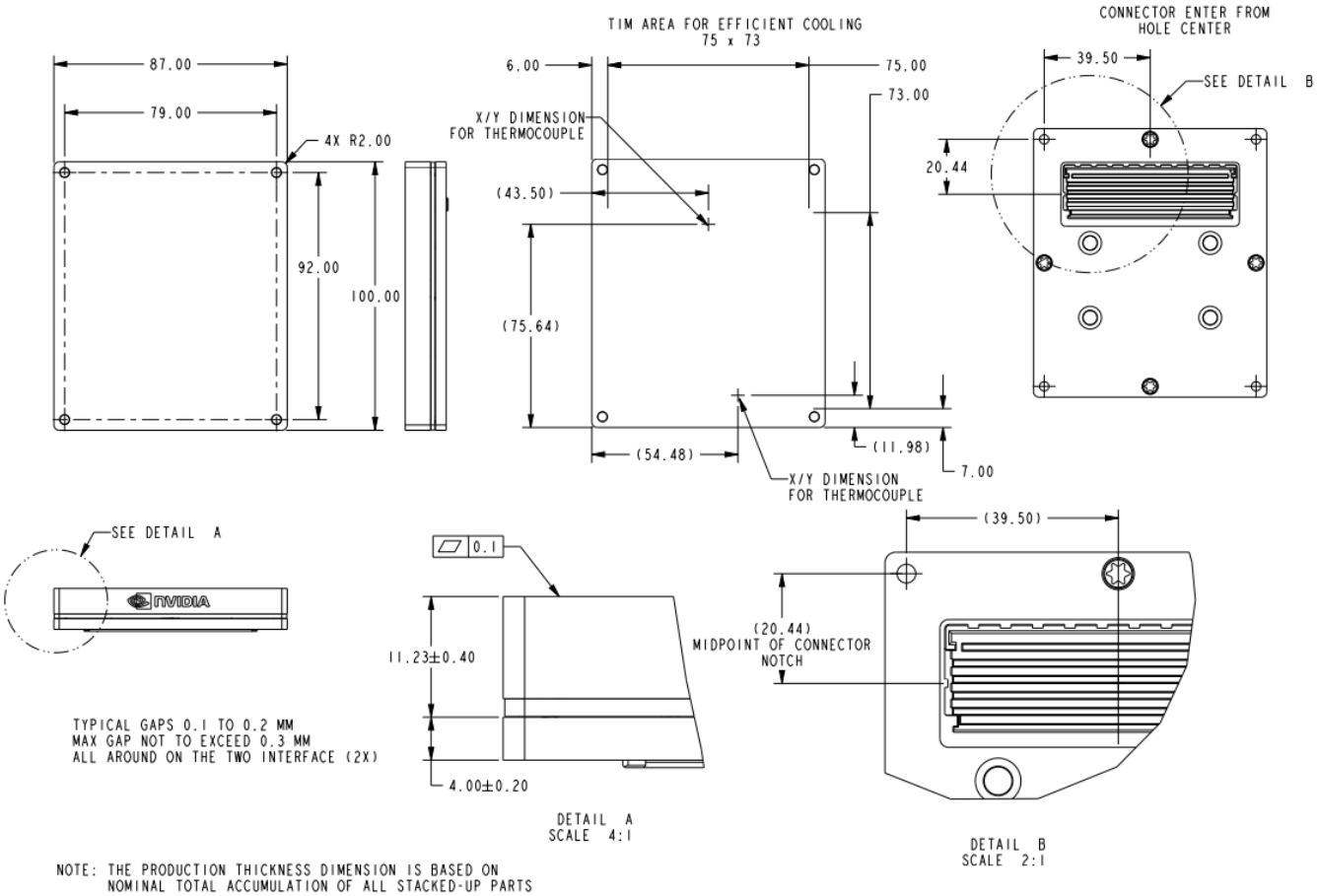
- Dimensions: 87 mm (width) x 100 mm (length) x 15.28 mm (height).
- Weight (module + TTP + bottom cover): 280 g (+/- 10 g)

All dimensions are in mm.

- PCB: 86.7 x 99.7 x 1.78* (+/- .267)
- TTP: 87 x 100 x 9.5 (Heatpipe / window TTP +/- 0.2)
- Bottom Cover: 87 x 100 x 4 (+/- 0.2)
- Board-to-board height: dependent on size of connector used on the carrier board; see the *Jetson AGX Xavier Series Product Design Guide* for more information

* 1.78 PCB Thickness: 1.62 +/- 0.167 solder mask to solder mask, 0.08 +/- 0.02 solder bumps PCB top, 0.08 +/- 0.08 solder bumps PCB bottom; solder bumps are based on stencil height, some will be crushed during assembly.

Figure 5 Module Outline Drawing



4.6 Module Marking

Laser etching. ECC 200 Barcode: Contains Device SN, MAC1 Address and Board Level Part Number(e.g., 0424617123456,00044BA4F228,699-82888-0004-400 – there is no space between SN, MAC1 and Part Number, only a comma)

Figure 6 JAX Module Marking

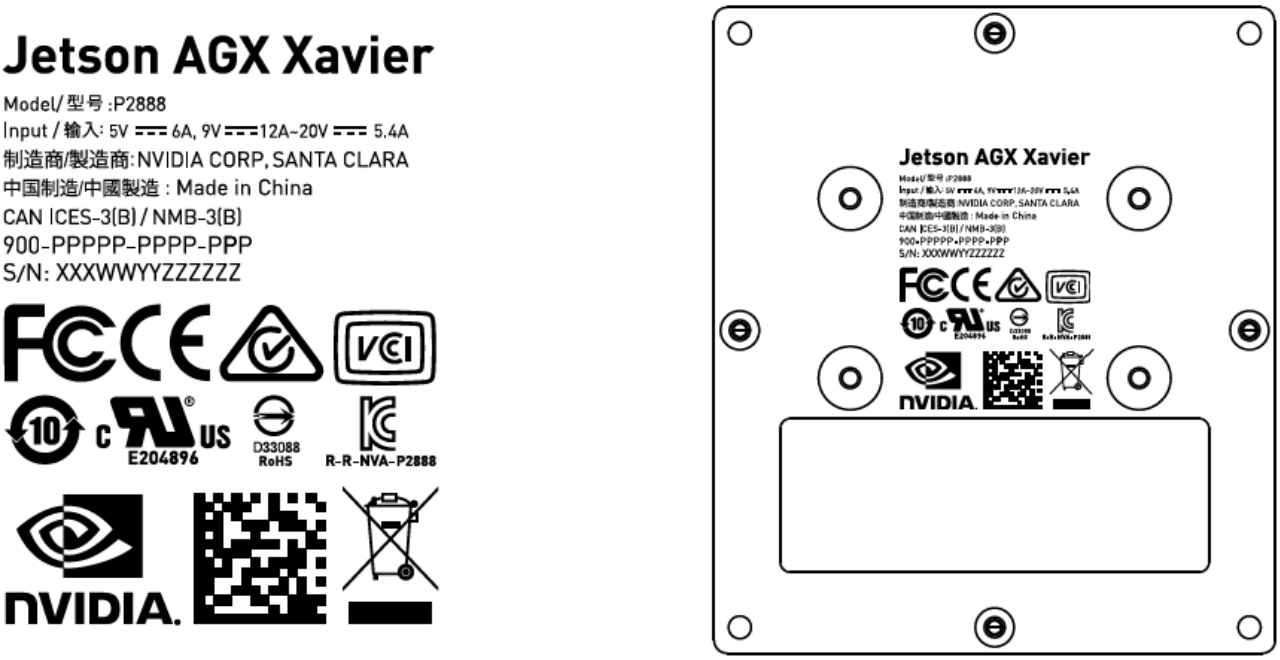
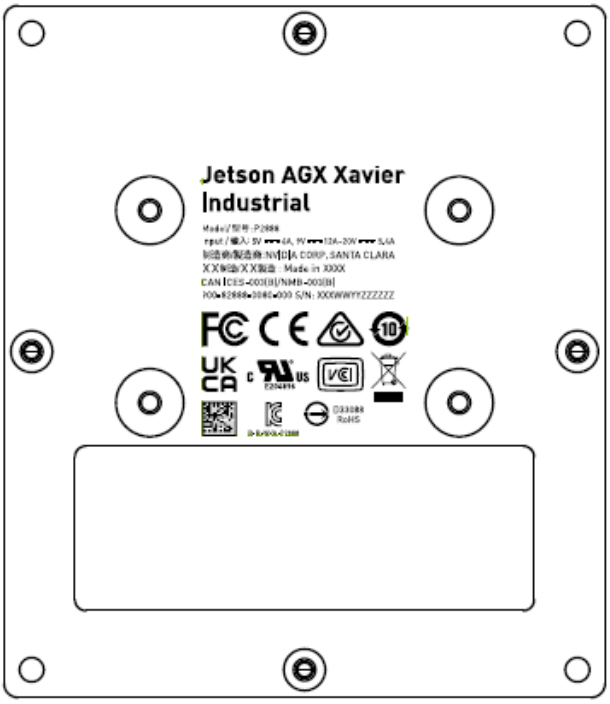


Figure 7 JAXi Module Marking



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