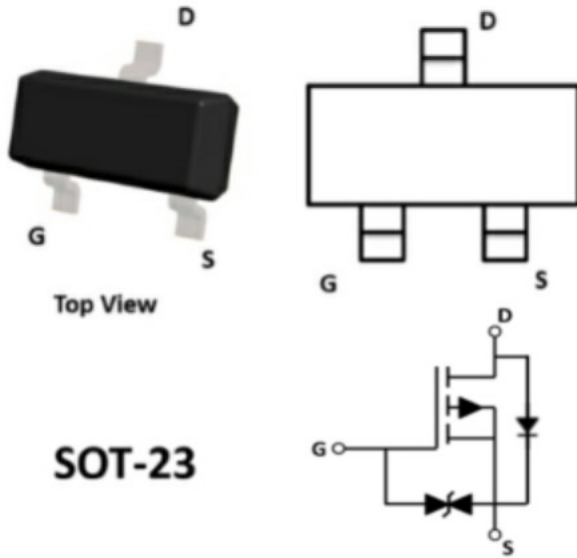


P-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} -20V
- I_D -0.65A
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <520 mohm
- $R_{DS(ON)}$ (at $V_{GS}=-2.5V$) <750 mohm
- ESD Protected Up to 4.5KV (HBM)

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Interfacing, Logic switch
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-20	V
Gate-source Voltage	V_{GS}	± 12	V
Drain Current	I_D	$T_A=25^\circ C$ Steady State	-0.65
		$T_A=70^\circ C$ Steady State	-0.52
Pulsed Drain Current ^A	I_{DM}	-2.6	A
Total Power Dissipation @ $T_A=25^\circ C$ Steady State	P_D	0.35	W
Thermal Resistance Junction-to-Ambient @ Steady State ^B	$R_{\theta JA}$	357	$^\circ C/W$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3139K	F2	39K.	3000	30000	120000	7" reel

YJL3139K

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V, T _C =25°C			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V		±1.5	±10	μA
		V _{GS} = ±8V, V _{DS} =0V		±500	±2000	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.35	-0.61	-1.2	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D =-0.6A		360	520	mΩ
		V _{GS} = -2.5V, I _D =-0.5A		570	750	
		V _{GS} = -1.8V, I _D =-0.3A		860	1300	
Diode Forward Voltage	V _{SD}	I _S =-0.65A, V _{GS} =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I _S				-0.65	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		71		pF
Output Capacitance	C _{oss}			20		
Reverse Transfer Capacitance	C _{rss}			15		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DD} =-10V, I _D =-0.65A		1.24		nC
Gate Source Charge	Q _{gs}			0.37		
Gate Drain Charge	Q _{gd}			0.27		
Reverse Recovery Charge	Q _{rr}	I _F =-0.5A, di/dt=-20A/us		0.97		
Reverse Recovery Time	t _{rr}			26		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-4.5V, V _{DD} =-10V, R _L =2.5Ω, R _{GEN} =3Ω		4		ns
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			16		
Turn-off Fall Time	t _f			25		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ Typical Performance Characteristics

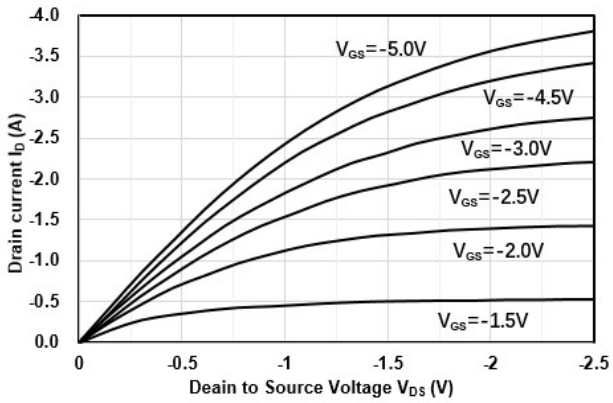


Figure1. Output Characteristics

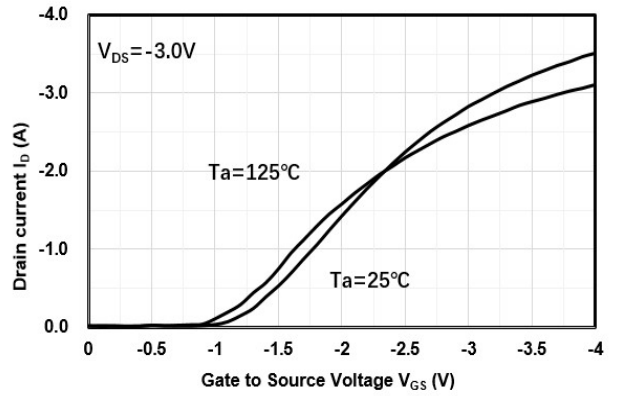


Figure2. Transfer Characteristics

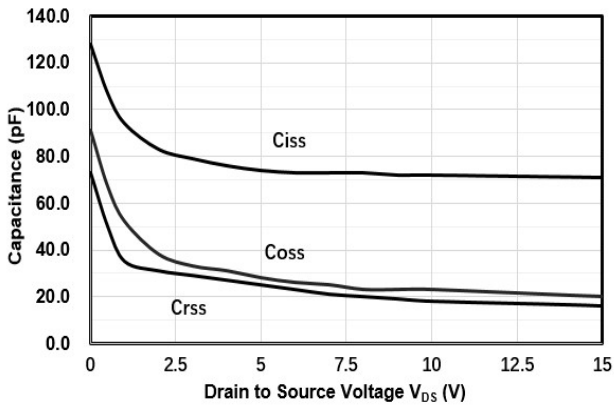


Figure3. Capacitance Characteristics

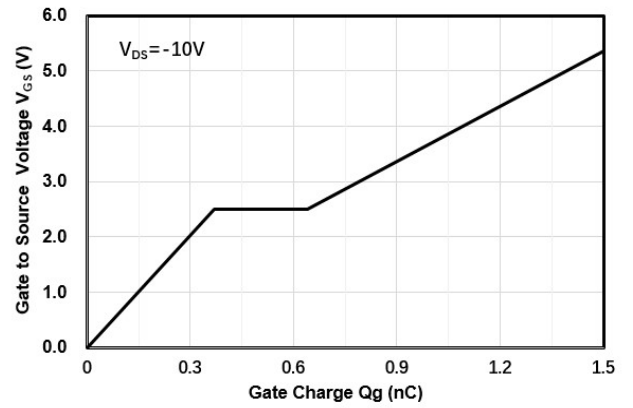


Figure4. Gate Charge

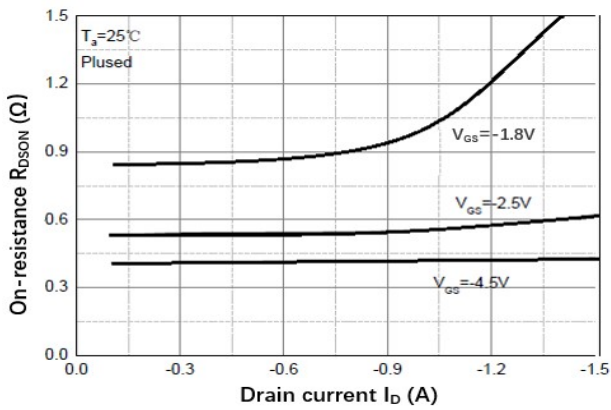


Figure5. Drain-Source on Resistance

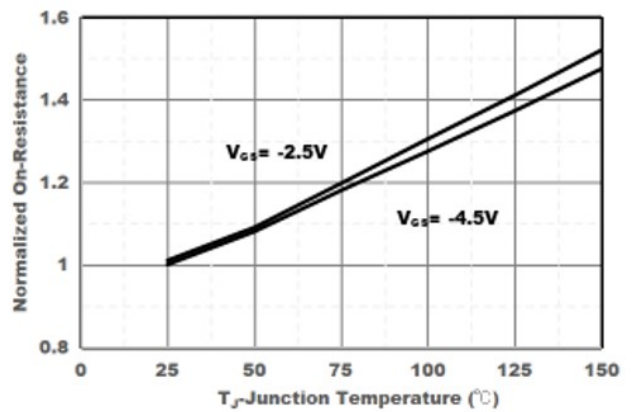
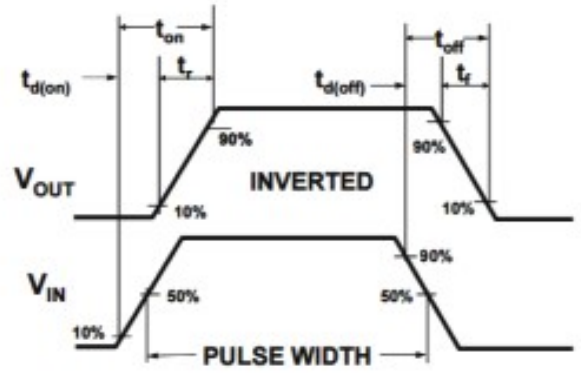
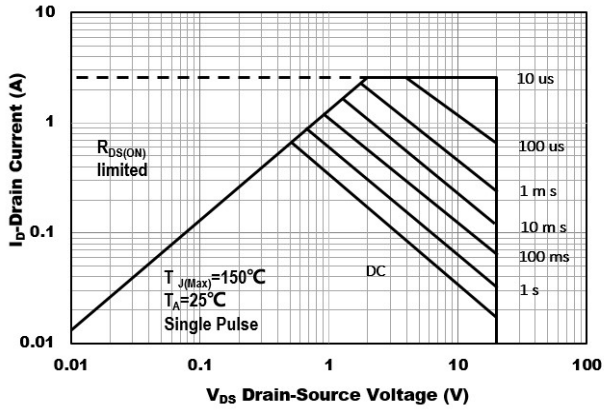
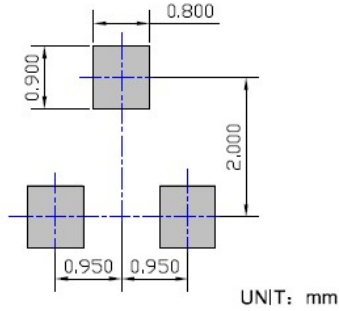
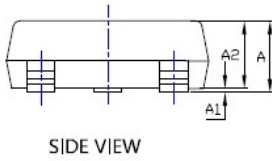
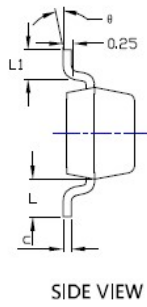
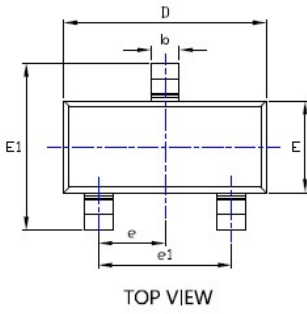


Figure6. Drain-Source on Resistance



YJL3139K

■ SOT-23 Package information



SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.035	---	0.045	0.900	---	1.150
A1	0.000	---	0.004	0.000	---	0.100
A2	0.035	0.038	0.041	0.900	0.975	1.050
b	0.012	0.016	0.020	0.300	0.400	0.500
c	0.004	---	0.008	0.100	---	0.200
D	0.110	0.114	0.118	2.800	2.900	3.000
E	0.047	0.051	0.055	1.200	1.300	1.400
E1	0.089	0.094	0.100	2.250	2.400	2.550
e	0.037TYP			0.950TYP		
e1	0.071	0.075	0.079	1.800	1.900	2.000
L	0.022REF			0.550REF		
L1	0.012	0.016	0.200	0.300	0.400	0.500
s	0*	---	8*	0*	---	8*

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

YJL3139K

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