LP3994

Wide Input Range High Performance LDO

Features

- Wide Input Voltage Range: 3.6V to 40V
- Maximum Load Current Up to 150mA
- Low Quiescent Current 1.5μA typical
- Low Dropout Voltage:
  - 550mV @ 100mA Load
  - 850mV @ 150mA Load
- Output Voltage Tolerance
  - ±1.5% @ 1mA Load
- Stable with Minimum 1.0μF Output Capacitance
- Short Circuit Current Limit 120mA
- Internal Thermal Overload Protection
- Excellent Load/Line Transient Response
- Line Regulation: 0.01%/V typical
- Load Regulation: 0.005%/mA typical
- ESD protections
- Package: SOT23-3, SOT23-5, SOT89-3
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Digital cameras
- Audio devices
- Portable and battery-powered equipment
- Post dc-to-dc regulation
- Post regulation

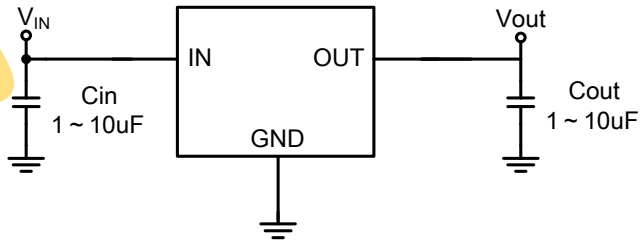
General Description

The LP3994 is a high performance low dropout（LDO）voltage regulator with wide input voltage range and low quiescent current (1.5μA typical). The device is suitable for a multitude of applications which require a regulated supply of up to 150mA load current. The device uses an advanced CMOS process and a PMOSFET to achieve fast start-up, high output voltage accuracy and excellent transient response performance.

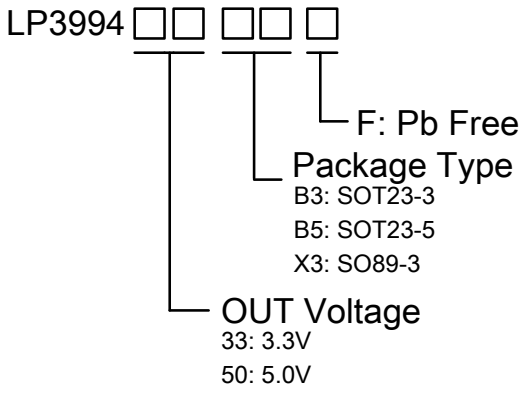
The LP3994 comes in standard fixed output voltage 3.3V and 5.0V. The device is stable with a 1.0μF~10μF ceramic output capacitor, The device is protected from short circuit by the current limit function and from over-heating by thermal overload protection.

The device is offered in SOT23-3，SOT23-5 ,SOT89-3 package.

Typical Application Circuit



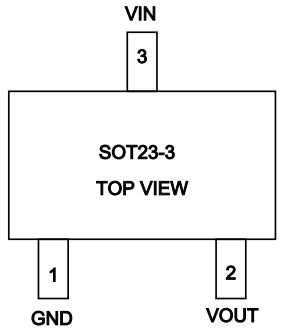
Order Information



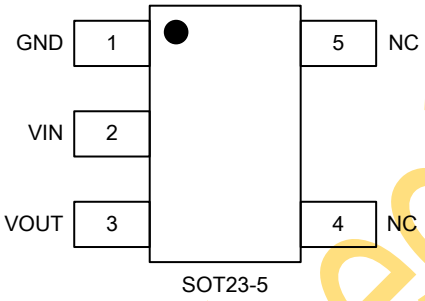
Device Information

Part Number	Top Marking	OUT Voltage	Moisture Sensitivity Level	Package	Shipping
LP3994-33B3F	LPS 3EYWX	3.3V	MSL3	SOT23-3	3K/REEL
LP3994-50B3F	LPS 3KYWX	5.0V	MSL3	SOT23-3	3K/REEL
LP3994-33B5F	LPS 3EYWX	3.3V	MSL3	SOT23-5	3K/REEL
LP3994-50B5F	LPS 3KYWX	5.0V	MSL3	SOT23-5	3K/REEL
LP3994-33X3F	LPS 3994 33WX	3.3V	MSL3	SOT89-3	1K/REEL
LP3994-50X3F	LPS 3994 50WX	5.0V	MSL3	SOT89-3	1K/REEL
LP3994B-33X3F	LPS 3994B 33WX	3.3V	MSL3	SOT89-3	1K/REEL
LP3994B-50X3F	LPS 3994B 50WX	5.0V	MSL3	SOT89-3	1K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.					

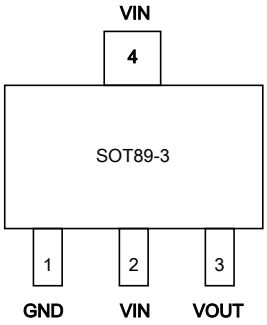
Pin Diagram



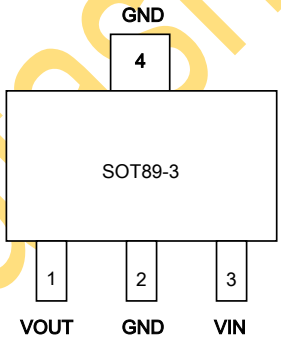
LP3994-XXB3F（top view）



LP3994-XXB5F（top view）



LP3994-XXX3F（top view）

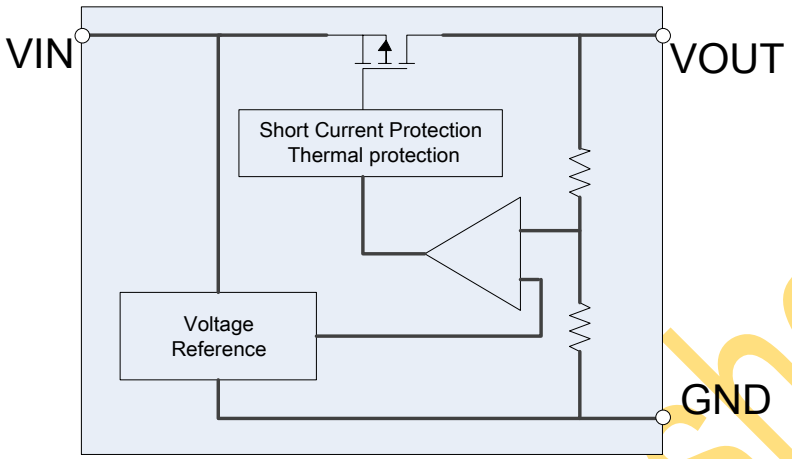


LP3994B-XXX3F（top view）

Pin Description

Pin				Name	Description
SOT23-3	SOT23-5	SOT89-3 (LP3994)	SOT89-3 (LP3994B)		
1	1	1	2, 4	GND	Ground.
2	3	3	1	VOUT	Output pin. Bypass a 1μF or greater ceramic capacitor from this pin to ground. Place the capacitor as close as to the pin.
3	2	2, 4	3	VIN	Supply input pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor. Place the capacitor as close as to the pin.
	4 , 5			NC	

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- IN Pin to GND ---------- -0.3 to 44V
- OUT Pin to GND ---------- -0.3 to 6V
- Maximum Junction Temperature (T_J) ---------- 150℃
- Maximum Power Dissipation(P_D) SOT23-3 @25℃---------- 0.5W
- Maximum Power Dissipation(P_D) SOT23-5 @25℃---------- 0.5W
- Maximum Power Dissipation(P_D) SOT89-3 @25℃---------- 0.7W
- Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85℃
- Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

- HBM(Human Body Model) ---------- 2KV
- MM(Machine Model) ---------- 200V

Recommended Operating Conditions

- Input Voltage ---------- 3.6V to 40V
- Operating Junction Temperature Range (T_J) ---------- -40℃ to 150℃
- Ambient Temperature Range ---------- -40℃ to 85℃
- Thermal Resistance θ_{JA} SOT23-3 ---------- 250℃/W
- Thermal Resistance θ_{JA} SOT23-5 ---------- 250℃/W
- Thermal Resistance θ_{JA} SOT89-3 ---------- 178℃/W

Electrical Characteristics

(The specifications are at T_A=25℃, V_{IN} = V_{OUT}+1V, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage operation Range		3.6		40	V
V_{DROP}	Dropout Voltage	V_{OUT}=3.3V, I_{LOAD}=100mA		550		mV
		V_{OUT}=3.3V, I_{LOAD}=150mA		850		
I_Q	DC Supply Quiescent Current	I_{LOAD}=0mA		1.5	2.5	μA
V_{OUT}	Output Voltage accuracy	I_{LOAD}=1mA	-1.5%	3.3 5.0	1.5%	V
Reg_{LINE}	Output Voltage Line Regulation	V_{IN}=V_{OUT}+1V~40V I_{LOAD}=10mA $\Delta V_{OUT}/\Delta V_{IN}/V_{OUT}$		0.01		%/V
Reg_{LOAD}	Output Voltage Load Regulation	I_{LOAD} from 1mA to 150mA V_{IN}=V_{OUT}+1V	10	17	25	mV
		I_{LOAD} from 1mA to 150mA LP3994-33B3F, V_{IN}=5V	10	18	42	
I_{LOAD}	Maximum Load Current	V_{IN}=V_{OUT}+1V	150			mA
I_{SHORT}	Short Current	OUT short to GND		120		mA
e_N	Output Noise	10Hz to 100kHz, I_{LOAD}=30mA		120		μV_{RMS}
T_{J_LIMIT}	Junction Temperature-Limit Protection			150		℃
PSRR	Power Supply Rejection Ratio	1kHz (C_{OUT}=1uF, I_{LOAD}=10mA)		-45		dB
T_{CVOUT}	V_{OUT} Temperature Coefficient			0.01		%/℃

Typical Characteristics

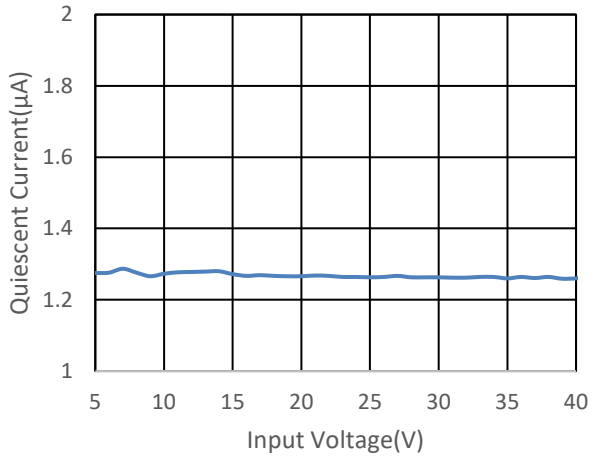


Figure 1. Quiescent Current vs input voltage, LP3994-33B3F, 25℃

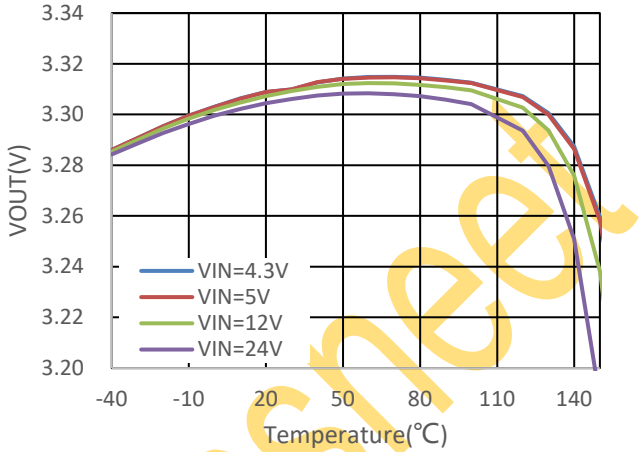


Figure 2. V_{OUT} vs Temperature, LP3994-33B3F, I_{LOAD}=1mA

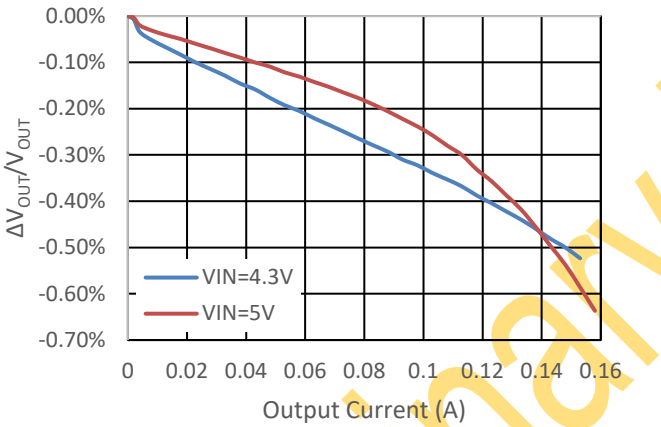


Figure 3. $\Delta V_{OUT}/V_{OUT}$ vs output current, LP3994-33B3F, 25℃

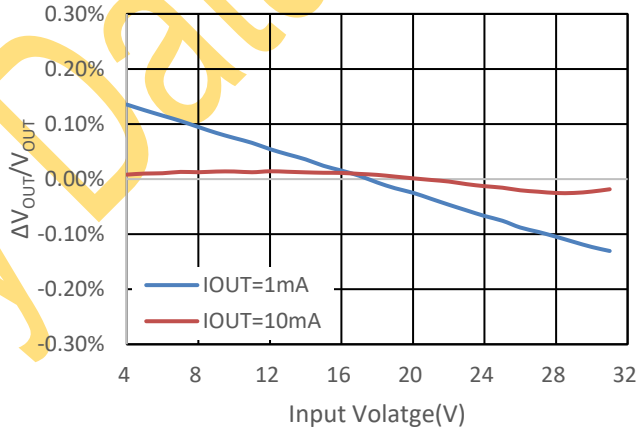


Figure 4. $\Delta V_{OUT}/V_{OUT}$ vs input voltage, LP3994-33B3F, 25℃

Detailed Description

Overview

The LP3994 is a low quiescent current, low dropout linear regulator which operates with fixed 3.3V and 5.0V output voltage and provides up to 150 mA output current. Drawing a low 1.5μA quiescent current makes the device ideal for battery-operated portable equipment. Optimized for use with the ceramic capacitors, the device provides excellent transient performance.

Internally, the LP3994 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

Short Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short to GND, the short current limit protection will be triggered and clamp the output current to approximately 120mA to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Overload Protection

Thermal overload protection is built-in, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output current capability will keep decreasing to make the temperature maintain to 150℃, which is the balance point between the temperature and the output current.

Low Dropout Voltage

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value. The LP3994 LDO has a very low dropout voltage specification of 850 mV (typical) at 150 mA of output current.

Application Description

Thermal Consideration

The reason which causes the lower output current capability of LP3994 device with high input voltage is the power dissipation of the device. Nearly all of the power dissipation is generated by the internal MOSFETs, the power dissipation can be calculated approximately:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Where P_D is the power dissipation.

The worst-case situation is when the device has the maximum input voltage 40V and maximum load current 150mA. In this situation, the device has to dissipate the maximum power.

$$P_{Dmax} = (40V - 3.3V) \times 150mA = 5.5W$$

This power dissipation of the LDO device in the SOT23-3 package will trigger thermal overload protection to decrease the output current capability. Then a trade-off must be made between the output current, cost and thermal requirements of the application.

Input Capacitor

Like all low dropout linear regulators, low-source impedance is necessary for the stable operation of the LDO. A 1μF-10uF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. Given the high input voltage capability of the LP3994, of up to 40V DC, it is recommended to use an appropriate voltage rating capacitor, and the derating of the capacitance as a function of voltage and temperature needs to be taken into account. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

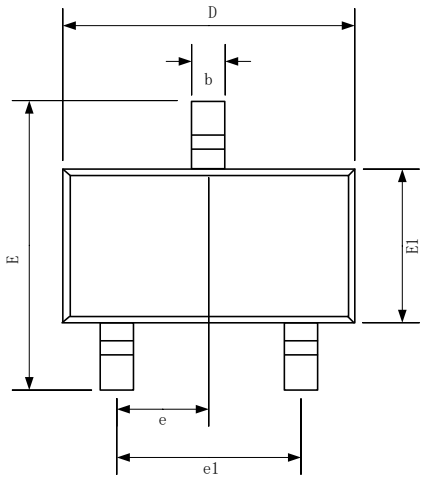
The LP3994 requires a minimum output capacitance of 1 μF for output voltage stability. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitor should be located as close to the LDO output as it is practical. It is recommended to use an appropriate voltage rating capacitor, and the derating of the capacitance as a function of voltage and temperature needs to be taken into account.

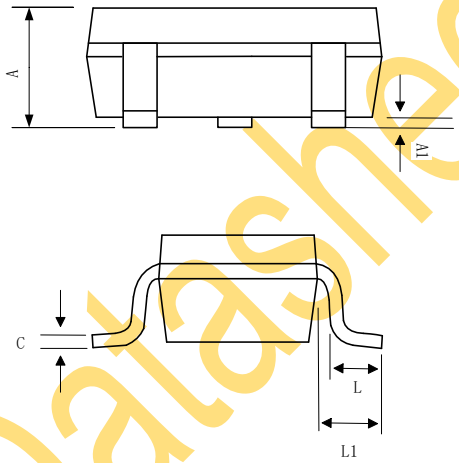
Layout Considerations

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes the inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device.

Packaging Information

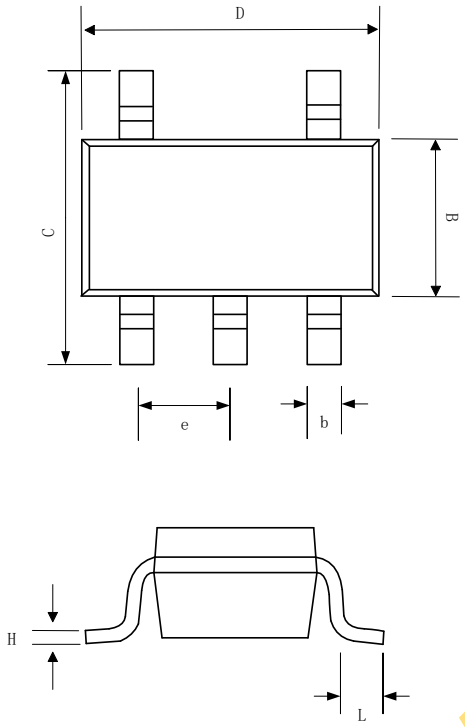
SOT23-3

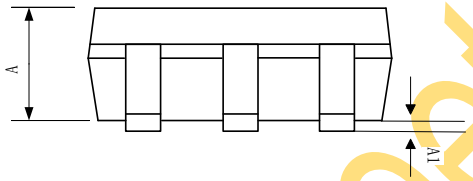


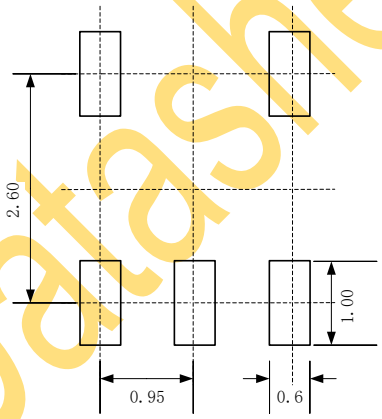


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.000	1.150	1.330
A1	0.000	0.050	0.130
b	0.300	0.380	0.450
c	0.110	0.150	0.190
D	2.820	2.920	3.020
E	2.600	2.800	3.000
E1	1.400	1.600	1.800
e	0.950BSC		
e1	1.900BSC		
L	0.300	0.450	0.600
L1	0.600REF		

SOT23-5



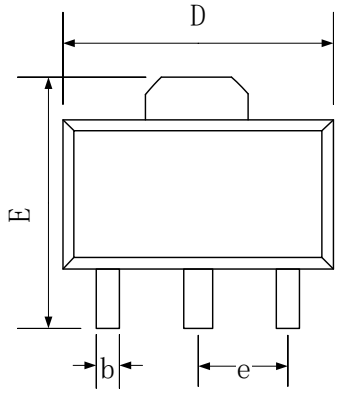




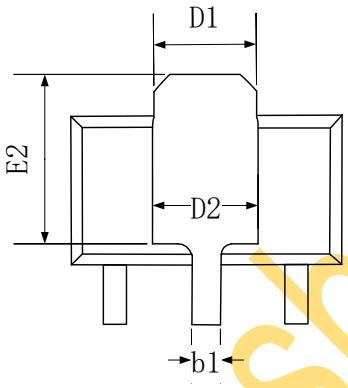
Recommended Land Pattern

SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

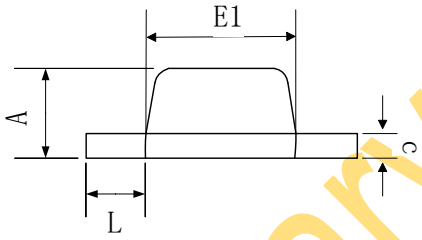
SOT89-3



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.40	1.50	1.60
b	0.32	0.42	0.52
b1	0.36	0.48	0.56
c	0.35	-	0.44
D	4.39	4.50	4.60
D1	1.55 REF		
D2	1.63 REF		
E	3.9	4.20	4.40
E1	2.30	2.45	2.60
E2	2.75 REF		
e	1.50 BSC		
L	0.78	1.00	1.20